Chapter 3

SYSTEM MODULE

CHAPTER 3 – TRANSCEIVER OVERVIEW

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Introduction

The TFE–1 model C is a radio transceiver unit for the GSM network. It is a GSM power class 4 transceiver providing 11 power levels with a maximum output power of 2W.

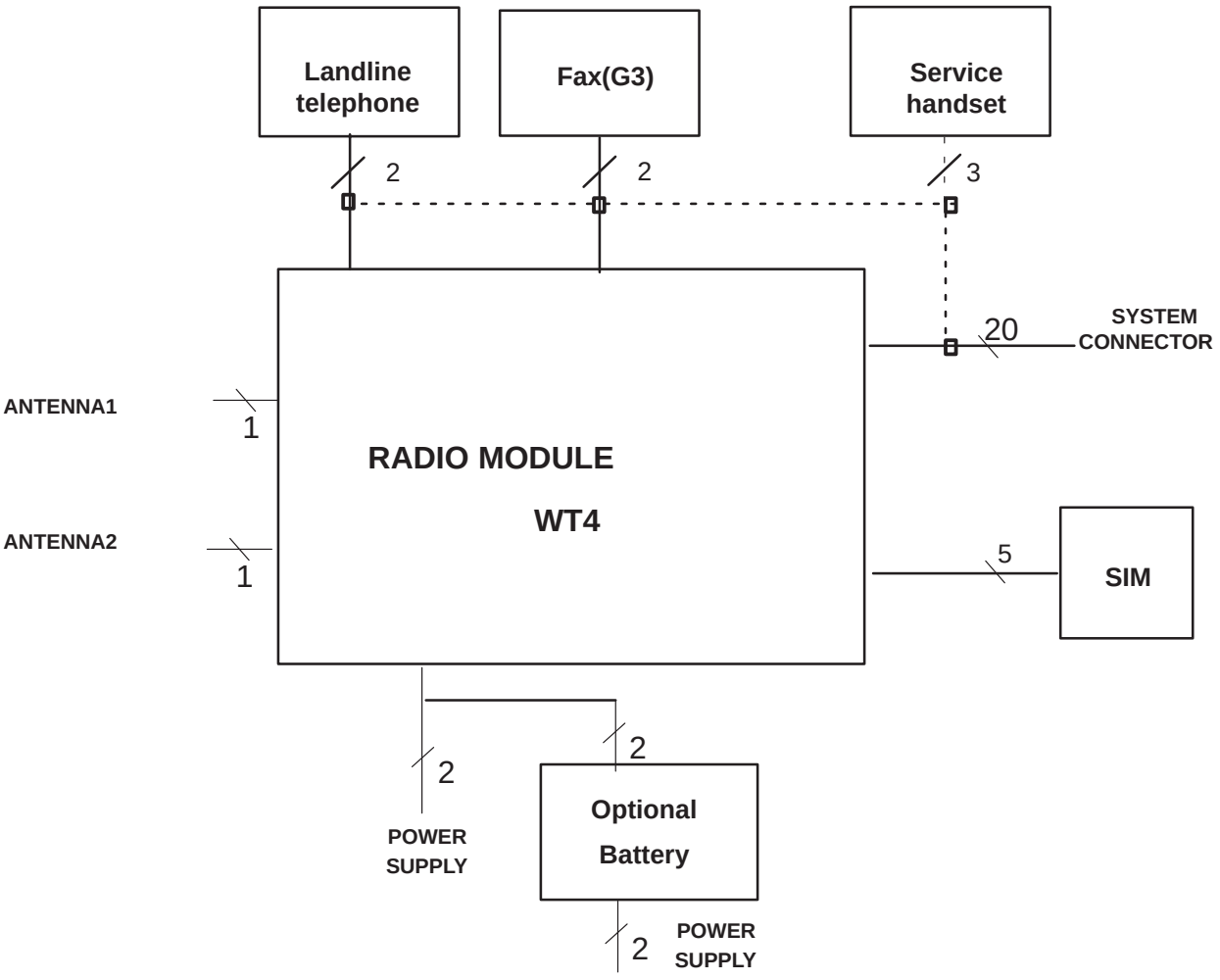
The transceiver consists of a Radio module (WT4C) and assembly parts

WT4C is the baseband/RF module TFE–1 model C cellular transceiver. The WT4C module carries out all the system and RF functions of the transceiver. System module WT4C is designed for a WLL terminal to operate in the GSM system.

Small–size SIM (Subscriber Identity Module) card is located inside the phone.

All functional blocks of the system module are mounted on a single multi layer printed circuit board. The chassis of the radio unit has separating walls for baseband and RF. The connections to accessories are taken through the system connector of the radio unit. There is no physical connector between the RF and baseband sections.

Block Diagram of External Connections



Modes of Operation

There are three different operation modes

– idle mode

– active mode

– local mode

In the idle mode transmitter is in OFF–stage.

In the active mode all the circuits are supplied with power although some parts might be in the idle state part of the time.

The local mode is used for alignment and testing.

Circuit Description

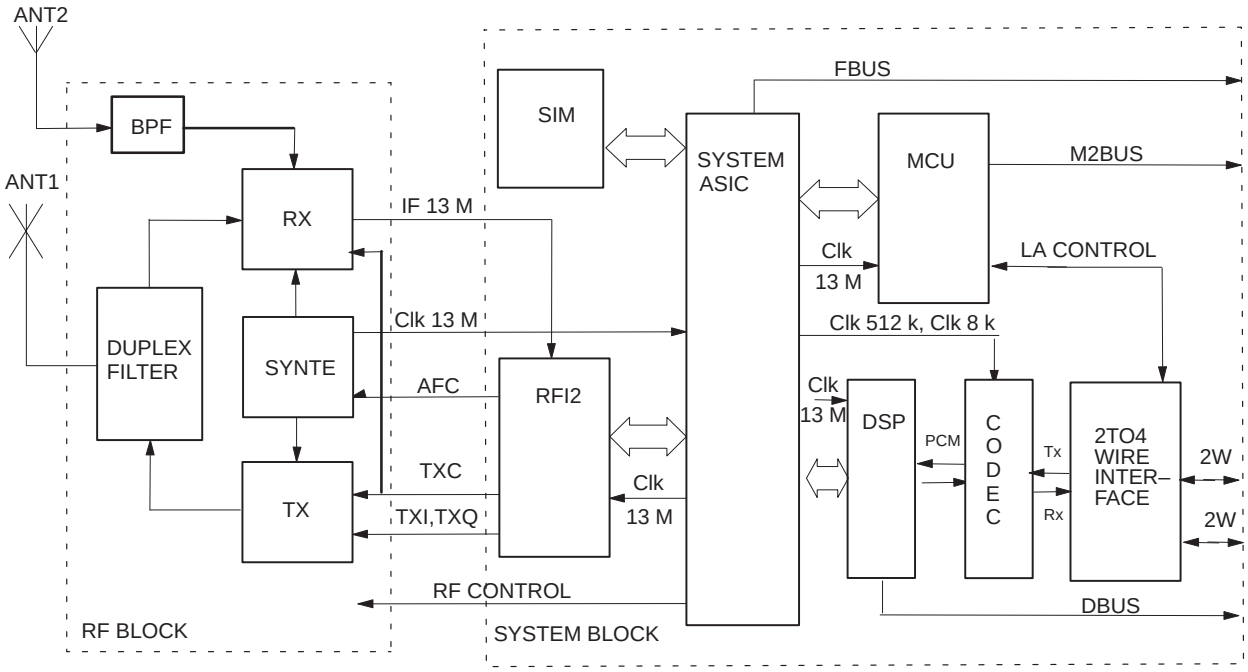
The transceiver electronics consists of one integrated Radio Module (RF + System blocks + LA block). System blocks, RF blocks and LA–block are interconnected with PCB wiring. Accessories are connected to the transceiver via a system connector or 2 RJ–11 connectors.

The System blocks provide the MCU and DSP environments, Logic control IC, memories, audio processing, RF control hardware (RFI2) and 2 to 4 wire interface for the landline telephone. On board power supply circuitry delivers operating voltages for both System and RF blocks. An on–board LA power unit generates feeding voltage and ringing voltage for the landline telephone.

The general purpose microcontroller, Hitachi H3001, communicates with the DSP, memories, and Logic control IC with an 16–bit data bus.

The RF block is designed for a WLL–terminal which operates in the GSM system. The purpose of the RF block is to receive and demodulate the radio frequency signal from the base station and to transmit a modulated RF signal to the base station.

Block Diagram



Power Distribution

The power supply is based on the ASIC circuit PSCLD. The chip consists of regulators and control circuits providing functions like automatic power up, reset and watchdog functions. External buffering is required to provide more current.

Automatic power up is needed because there is no ‘power on‘ –button on the terminal so whenever power supply is connected to the terminal it will start automatically the power up procedure. If the input voltage is too high or too low, the terminal will automatically shut off, and when the voltage is in the correct window, it will automatically start power–up procedure.

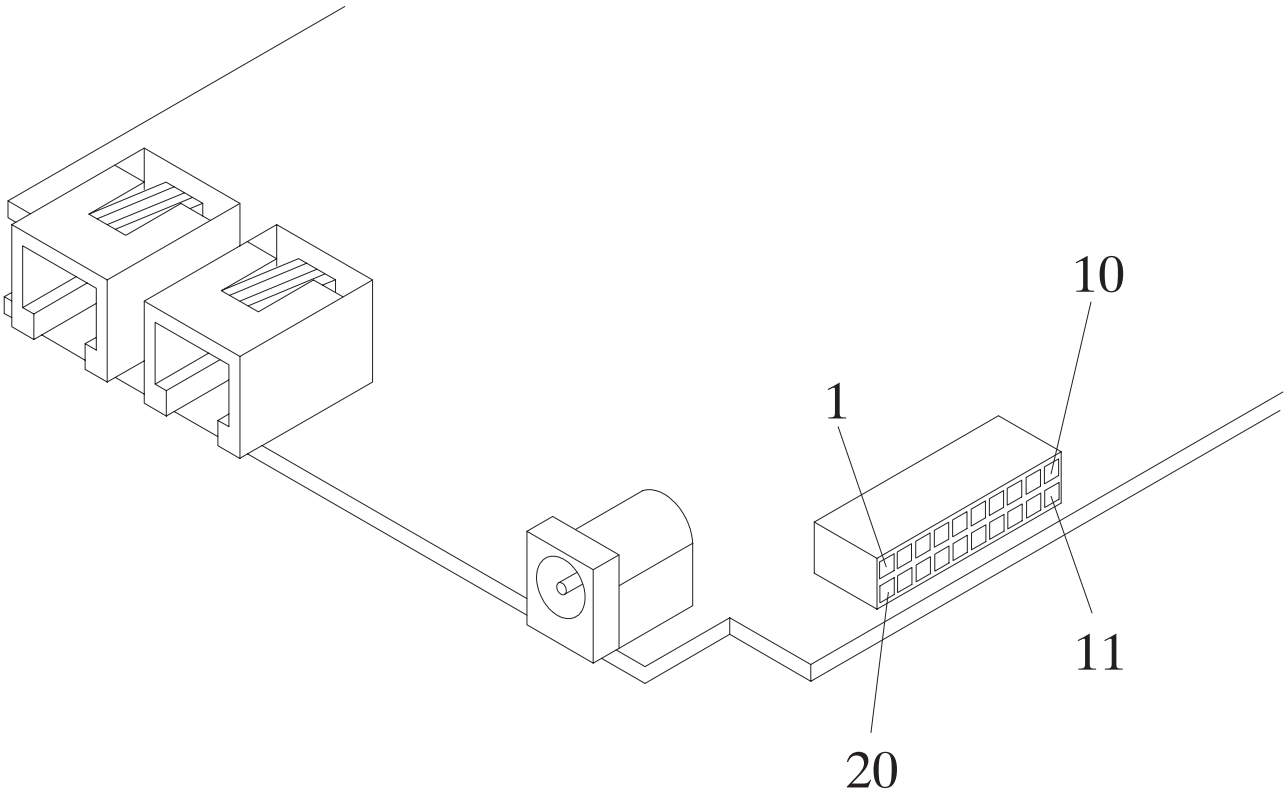
Charging control is not supported.

The detailed power distribution diagrams are given in Baseband blocks and RF blocks documents.

External Connections

The system module has two connectors, an external system connector, and SIM connector.

System Connector X120



Accessory Connector

Pin:	Name:	Description:
1	RS_RX	Serial RX (Receive data for serial communica–tion) • ”0”; min/max 0...0.6 V • ”1”; min/max 2.4...3.2 V
2	RS_TX	Serial TX (Transmit data for serial communica–tion) • ”0”; min/max 0...0.6 V • ”1”; min/max 2.4...3.2 V
3	SCK_RTS	Serial Clock (Serial Clock for synchronous communication / RS_RTS) • ”0”; min/max 0...0.6 V • ”1”; min/max 2.4...3.2 V
4	WDDIS	• ”0”; min/max 0...0.6 V Watchdog disable, Flash mode • ”1”; min/max 2.4...7.15 V, Normal mode
5	PCMDCLK	Audio Clock (512 kHz) clock for audio data • ”0”; min/max 0...0.6 V • ”1”; min/max 2.4...3.2 V
6	MBUS	Serial control bus (General Purpose Control and Test Control Bus) • ”0”; min/max 0...0.5 V • ”1”; min/max 2.4...3.2 V
7	VPP	Programming Voltage (Programming voltage is applied before entering the programming state) • active; min/max 11.6...12.6 V • inactive; min/max 0...3.2 V
8	DBUS_RXD	DBUS Interface (Receive data for DAI) • ”0”; min/max 0...0.6 V • ”1”; min/max 2.4...3.2 V
9	DBUS_TXD	DBUS Interface (Transmit data for DAI) • ”0”; min/max 0...0.6 V • ”1”; min/max 2.4...3.2 V
10	PCMSCLK	Audio Clock (8 kHz slot clock for audio data) • ”0”; min/max 0...0.6 V • ”1”; min/max 2.4...3.2 V
11	VL	Logic Supply Voltage (3 V Logic voltage) • typical; 3.2 V
12	FBUS_TX	FBUS TX (FBUS transmit) • ”0”; min/max 0...0.5 V • ”1”; min/max 2.4...3.2 V

Pin:	Name:	Description:
13	FBUS_RX	FBUS RX • FBUS receive ”0”; min/max 0...0.6 V • Pull–up on base band ”1”; min/max 2.4...3.2 V
14	VBATT	Battery supply voltage • min/max 6.0...6.9 V
15	DGND	Digital ground
16	RS_CTS	RS232 (Handshake signal for RS–232 serial interface)
17	HOOK_DTR	Accessory detection • active; min/max 0...0.5 V • inactive; min/max 2.4...3.2 V
18	AGND	Analog ground
19	XMIC_ID	External Microphone Input (Audio in e.g. service handset) • typical 200 mV
20	XEAR_DSR	External Speaker (Audio out e.g. service handset)

SIM Connector X300

Pin:	Name:	Description:
4	GND	Ground for SIM
1	VSIM	SIM voltage supply • min/typ/max: 4.8...4.9...5.0 V
6	SDATA	Serial data for SIM
2	SRES	Reset for SIM
3	CLK	Clock for SIM data (clock frequency minimum 1 MHz if clock stopping not allowed)

Baseband Block

Introduction

The WT4C module is used in TFE–1 model C products. The baseband is built around one DSP, System ASIC and the MCU. The DSP performs all speech and GSM/PCN related signal processing tasks. The baseband power supply is 3V, except for the A/D and D/A converters that are the interface to the RF section, and to the comparators in the LAPWRU.

The audio codec is a separate device which is connected to both the DSP and the MCU. The audio codec supports the internal audio from line adapter and external audio from the service handset.

The baseband clock reference is derived from the RF section, and the reference frequency is 13 MHz. A low level sinusoidal wave form is fed to the ASIC which acts as the clock distribution circuit. The DSP is running at 39 MHz using an internal PLL. The clock frequency supplied to the DSP is 13 MHz. The MCU bus frequency is the same as the input frequency. The system ASIC provides both 13 MHz and 6.5 MHz as alternative frequencies. The MCU clock frequency is programmable by the MCU. The baseband uses 13 MHz as the MCU operating frequency. The RF A/D, D/A converters are operated using the 13 MHz clock supplied from the system ASIC

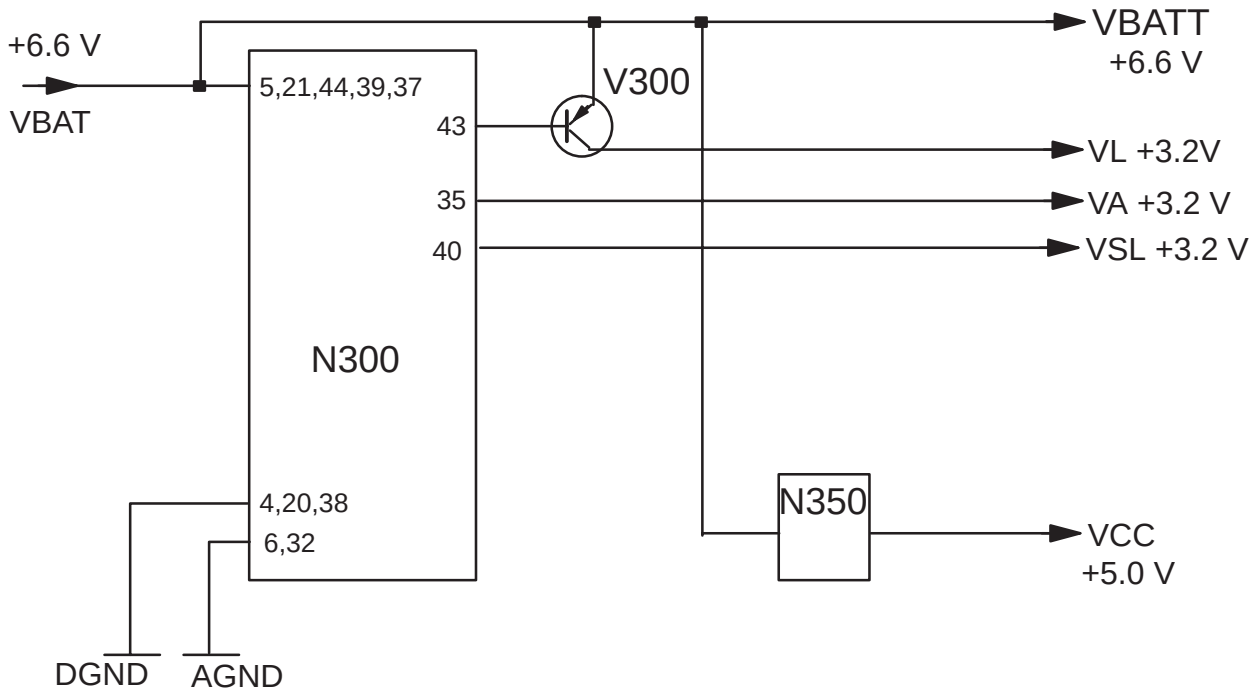
The power supply IC contains three different regulators. The output voltage from each regulator is 3.15V nominal. One of the regulators uses an external transistor as the boost transistor.

Modes of Operation

The baseband can operate only in the active mode in WLL terminal.

Circuit Description

Power Supply



The baseband has one power supply circuit N300 delivering power to the different parts in the baseband. There are two logic power supplies and one analog power supply. The analog power supply VA is used for analog circuits such as audio codec. Due to the current consumption and the baseband architecture the digital supply is divided into to parts.

Both digital power supply VSL and VL from the N300 PSCLD are used to distribute the power dissipation inside N300 PSCLD. The main logic power supply VL has an external power transistor, V300 to handle the power dissipation.

D400, ASIC, and the MCU SRAM D440 are connected to the same logic supply voltage. All other digital circuits are connected to the main digital supply. The analog voltage supply is connected to the audio codec.

Power Supply Regulator PSCLD, N300

The power supply regulators are integrated into the same circuit N300. The power supply IC contains three different regulators. The main digital power supply regulator is implemented using an external power transistor V300. The other two regulators are completely integrated into N300.

PSCLD, N300 External Components

N300 performs the required power–on timing. The PSCLD N300 internal power on and reset timing is defined by the external capacitor C318. This capacitor determines the internal reset delay, which is applied when the PSCLD N300 is initially powered by applying the power supply. The baseband power–on delay is determined by C315. With a value of 10 nF, the power–on delay after a power–on request has been active is in the range of 50–150 ms. C311 determines the PSCLD N300 internal oscillator frequency, and the minimum power–off time when power is switched off.

The sleep control signal from the ASIC D400 is connected via PSCLD N300. During normal operation, the baseband sleep function is controlled by the ASIC D400, but since the ASIC is not powered up during the startup phase, the sleep signal is controlled by PSCLD N300 as long as the PURX signal is active. This arrangement ensures that the 13 MHz clock provided from RF to the ASIC D400 is started and stable before the PURX signal is released, and the baseband exits reset. When PURX is inactive high, the sleep control signal is controlled by the ASIC D400.

N300 requires capacitors on the input power supply as well as on the output from each regulator to keep each regulator stable during different load and temperature conditions. Due to EMC precautions, a filter using C301, L302 and L303 has been inserted into the supply rail. This filter reduces the high frequency components present at the VBAT from exiting the baseband into the power supply. The regulator outputs also have filter capacitors for power supply filtering and regulator stability. A set of different capacitors are used to achieve a high bandwidth in the suppression filter.

PSCLD, N300 Control Bus

The PSCLD N300 is connected to the baseband common serial control bus. This bus is a serial control bus from the ASIC D400 to several devices on the baseband. This bus is used by the MCU to control the operation of N300 and other devices connected to the bus. N300 has two internal 8 bit registers and the PWM register used for charging control. The registers contain information for controlling reset levels, charging HW limits, watchdog timer length, and watchdog acknowledgement.

The control bus includes three wires: clock, serial data, and chip select for each device on the bus. From the PSCLD N300 point of view, the bus can be used for writing only. It is not possible to read data from PSCLD N300 using this bus.

The MCU can program the HW reset levels when the baseband exits/enters reset. The programmed values are retained until PSCLD N300 is powered off, i.e. the power supply is cut off. At initial power–on, when PSCLD is powered–on, the default reset level is used. The default value is 5.1 V, with the default hysteresis of 400 mV. This means that reset is exit at 5.5 V when the PSCLD N300 is powered for the first time.

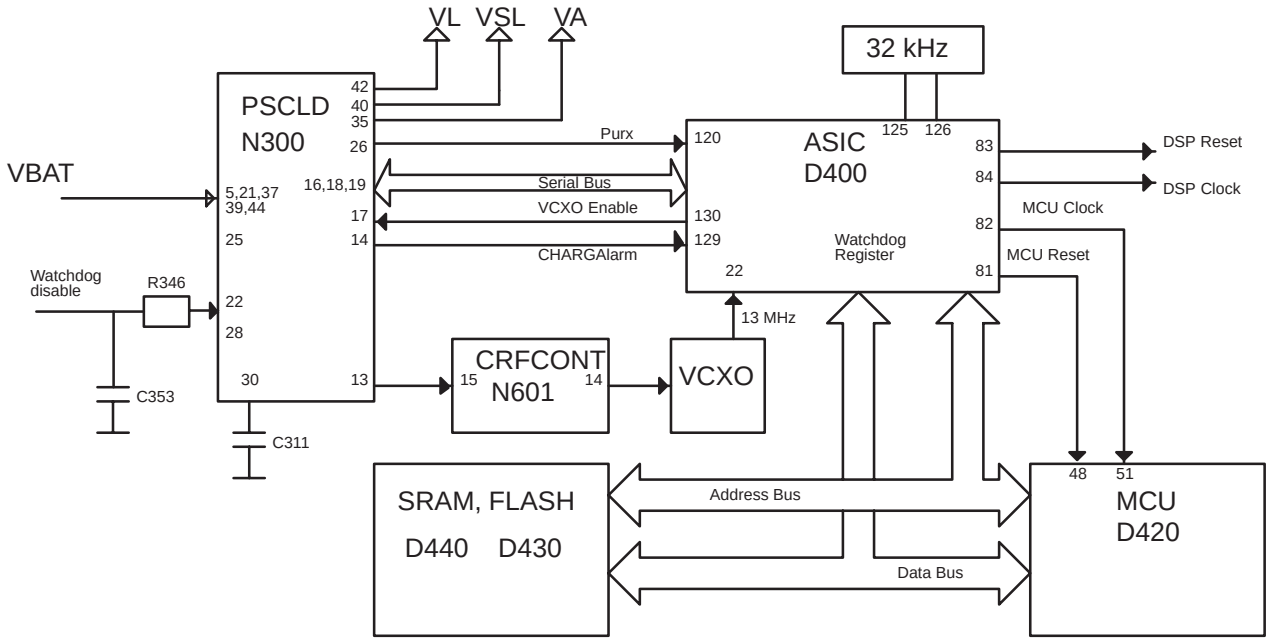
The watchdog timer length can be programmed by the MCU using the serial control bus. The default watchdog time is 32 s with a 50 % tolerance. The complete baseband is reset if the watchdog is not acknowledged within the specified time. The watchdog is running while PSCLD N300 is powering–up the system but PURX is active. This arrangement ensures that if for any reason the supply voltage doesn't increase above the reset level within the watchdog time the system is reset by the watchdog. As the time PURX is active is not exactly known, and depends upon startup conditions, the watchdog is internally acknowledged in PSCLD when PURX is released. This allows the MCU always the same time to respond to the first watchdog acknowledgement.

The PSCLD N300 also contains a switch for connecting and the supply voltage to the baseband A/D converters. The switch state can be changed by the MCU via the serial control bus. When PURX is active, the switch is open to prevent the supply voltage from being applied to the baseband measurement circuitry, which is powered off. Before any measurement can be performed, the switch must be closed by MCU.

SIM Interface and Regulator in N300

The SIM card regulator and interface circuit is integrated into PSCLD N300. The benefit from this is that the interface circuits are operating from the same supply voltage as the card, avoiding the voltage drop caused by the external switch used in previous designs. The PSCLD N300 SIM interface also acts as voltage level shifting between the SIM interface in the ASIC D400 operating at 3V and the card operating at 5V. Interface control in PSCLD is direct from ASIC, D400 SIM interface. The MCU can select the power supply voltage for the SIM using the serial control bus. The default value is 3V which needs to be changed to 5V before power–up of the SIM interface in ASIC D400. The regulator enable and disable is controlled by the ASIC via SIMI(2).

Power–Up Sequence



Power–On Reset Operation

The system power–up reset is generated by the regulator IC N300. The reset is connected to the ASIC D400 that is reset whenever the reset signal PURX is low. The ASIC D400 then resets the DSP D360, the MCU D420, and the digital parts in N450. When reset is removed, the clock supplied to the ASIC D400 is enabled inside the ASIC. At this point, the 32 kHz oscillator signal is not enabled inside the ASIC, since the oscillator is still in the startup phase. To start up the block requiring 32 kHz clock, the MCU must enable the 32 kHz clock. The MCU reset counter is now started and the MCU reset is still kept active low. A 6.5 MHz clock is started to MCU in order to put the MCU D420 into reset. The MCU is a synchronous reset device, and needs a clock to reset. The reset to MCU is set inactive after 128 MCU clock cycles, and MCU is started.

DSP D360 and N450 reset is kept active when the clock inside the ASIC D400 is started. A13 MHz clock is started to DSP D360 and puts it into reset. D360 is a synchronous reset device, and requires a clock to enter reset. The N450 digital parts are reset asynchronously and do not need a clock to be supported to enter reset.

As both the MCU D420 and DSP D360 are synchronous reset devices, all interface signals connected between these devices and ASIC D400 which are used as I/O are set into input mode on the ASIC D400 side during reset. This avoids bus conflicts occurring before the MCU D420 and the DSP D360 are actually reset.

The DSP D360 and N450 reset signal remains active after the MCU has exited reset. The MCU writes to the ASIC register to disable the DSP reset. This arrangement allows the MCU to reset the DSP D360 and N450 whenever need-

ed. The MCU can put DSP into reset by writing the reset active in the ASIC D400 register

MCU

The baseband uses a Hitachi H3001 type of MCU. This is a 16–bit internal MCU with 8–bit external data bus. The MCU is capable of addressing up to 16 MByte of memory space linearly, depending upon the mode of operation. The MCU has a non multiplexed address/data bus which means that memory access can be done using less clock cycles thus improving the performance but also tightening up memory access requirements. The MCU is used in mode 3 which means 8–bit external data bus and 16 Mbyte of address space. The MCU operating frequency is equal to the supplied clock frequency. The MCU has 512 bytes of internal SRAM. The MCU has one serial channel, USART that can operate in synchronous and asynchronous mode. The USART is used in the MBUS implementation. The clock required for the USART is generated by the internal baud rate generator. The MCU has 5 internal timers that can be used for timing generation. Timer TIOCA0 input pin 71 is used for generation of the netfree signal from the MBUS receive signal which is connected to the MCU USART receiver input on pin 2.

The MCU contains 4 10–bit A/D converters channels that are used for baseband monitoring.

The MCU, D420 has several programmable I/O ports which can be configured by SW. In this case, the data bus lines D0–D7 are used for baseband control functions. It is not used as part of the data bus.

MCU Access and Wait State Generation

The MCU can access external devices in 2 state access or 3 state access. In two state access the MCU uses two clock cycles to access data from the external device In 3 state access the MCU uses 3 clock cycles to access the external device or more if wait states are enabled. The wait state controller can operate in different modes. In this case, the programmable wait mode is used. This means that the programmed amount of wait states in the wait control register are inserted when an access is performed to a device located in that area. The complete address space is divided into 8 areas each area covering 2 MByte of address space. The access type for each area can be set by bits in the access state control register. Furthermore, the wait state function can be enabled separately for each area by the wait state controller enable register.

This means that in 3 state access, two types of access can be performed with a fixed setting:

– 3 state access without wait states

– 3 state access with the amount of wait states inserted determined by the wait control register

If the wait state controller is not enabled for a 3 state access area, no wait states are inserted when accessing that area even if the wait control register contains a value that differs from 0 states.

MCU Flash Loading

The flash loading equipment is connected to the baseband by means of the service adapter. The power supply for the baseband is supplied via the adapter and controlled by the flash programming equipment. The baseband module is powered up when the power is connected to the power supply connector.

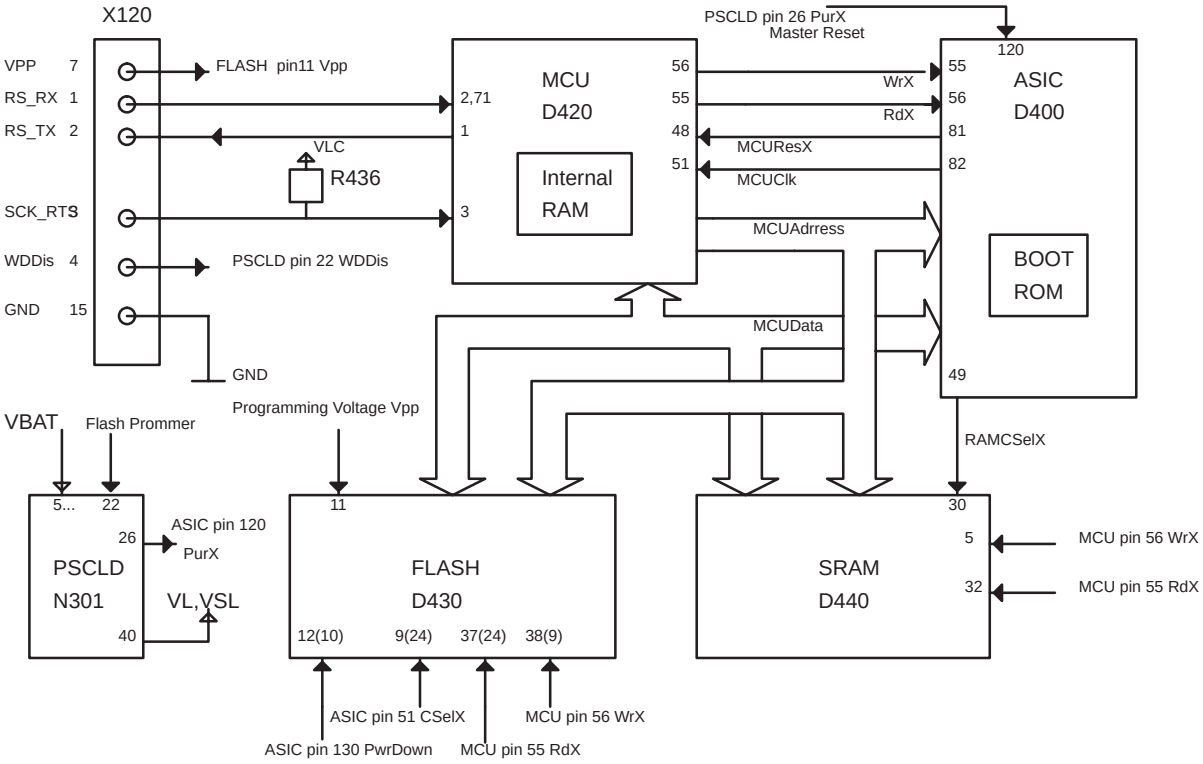
Five signals are required for the flash programming, with the addition of the power supply. The baseband MCU will automatically wait for flash down–loading to be performed if one of the two following criteria are met.

– The flash is found to be empty when tested by the MCU

– The serial clock line at the baseband MCU is forced low when the MCU is exiting reset

The second alternative is used for reprogramming as the flash is not empty in this case. To allow the serial clock line to be forced low during MCU initial boot there is a requirement that the flash prommer can control the power on of the baseband module. This is done by controlling the switching of the power supply. This arrangement allows the baseband module to operate in normal mode even if the flash prommer is connected but not active. The flash prommer also disables the power supply watchdog during flash programming to prevent unwanted reset of the baseband. The programming voltage to the flash is applied when the flash prommer has detected that the baseband module is powered. This detection is performed by monitoring the serial interface RS_RX line from the baseband. The RS_RX line is pulled high by a pull–up resistor in idle. The VPP voltage is set to 5V as it is not known at this point what type of device is used.

The following diagram shows the block diagram for the baseband flash programming circuitry.

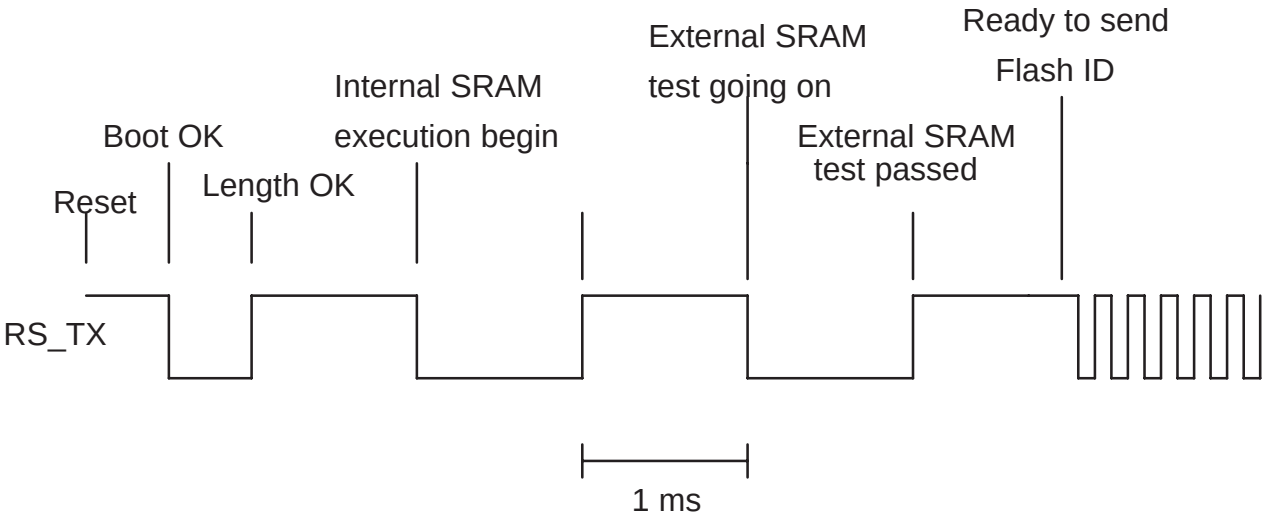


The interface lines between the flash prommer and the baseband are in low state when power is not connected by the flash prommer. The data transfer between the flash programming equipment and the base band is synchronous, and the clock is generated by the flash prommer. The same MCU USART that is used for MBUS communication is used for the serial synchronous communication. The PSCLD watchdog is disabled when the service adapter and flash prommer are connected.

After the service adapter has been connected to the board the power to the baseband module can be connected by the flash prommer or the test equipment. All interface lines are kept low, except for the data transmit from the baseband that is in reception mode on the flash prommer side, this signal is called RS_TX. The MCU boots from ASIC and investigates the status of the synchronous clock line. If the clock input line from the flash prommer is low or no valid SW is located in the flash, MCU forces the initially high RS_TX line low acknowledging to the flash prommer that it is ready to accept data.

The flash prommer sends data length, 2 bytes, on the RS_RX data line to the baseband. The MCU acknowledges the 2 data byte reception by pulling the RS_TX line high. The flash prommer now transmits the data on the RS_RX line to the MCU. The MCU loads the data into the internal SRAM. After having received the transferred data correctly MCU puts the RS_TX line low and jumps into internal SRAM and starts to execute the code. After a guard time of 1 ms the RS_TX line is put high by the MCU. After 1 ms the RS_TX is put low indicating that the external SRAM test is going on. After a further 1 ms, the RS_TX is put high indicating that external SRAM test has passed. The MCU performs

the flash memory identification based upon the identifiers specified in the Flash Programming Specifications. In case of an empty device, identifier locations shows FFH, the flash device code is read and transmitted to the Flash Prommer.



After that, the device mounted on baseband has been identified, and the Flash Prommer down–loads the appropriate algorithm to the baseband. The programming algorithm is stored in the external SRAM on the baseband module, and after having down–loaded the algorithm and data transfer SW, the MCU jumps to the external SRAM and starts to execute the code.

The MCU now asks the prommer to connect the flash programming power supply. This SW loads the data to be programmed into the flash, and implements the programming algorithm that has been down loaded.

Flash, D430

A 8 MBit Boot Block flash is used as the main program memory D430. The device is 3 V read/program with external 12V VPP for programming. The device has a lockable boot sector. This function is not used since the complete code is reprogrammed. The Boot sector is located at the ”bottom”, definition by Intel, address 00000H–03FFFH. The block is unlocked by a logic high state on pin 12. This logic high level is generated from VPP. The device can be programmed by a VPP of 5V but the programming procedure takes longer. To improve programming, the programming voltage used is 12V. The speed of the device is 150 ns. The MCU operating at 6.5 MHz will access the flash in 2 state access, requiring 150 ns access time from the memory.

SRAM D440

The baseband is designed to take two different size of SRAMs, 64kx8 and 128kx8, not at the same time. The required speed is 150 ns as the MCU will operate at 6.5 MHz and the SRAM will be accessed in 2 state access. The SRAM has no battery backup which means that the content is lost even during

short power supply disconnections. As shown in the memory map, the SRAM is not accessible after boot until the MCU has enabled the SRAM access by writing to the ASIC register.

EEPROM D445

The baseband is designed to take an 2kx8 serial EEPROM. TFE–1 model C will use the 2kx8 serial device over the I2C bus. The I2C bus protocol is implemented in SW and the physical implementation is performed on MCU Port 4.

MCU and Peripherals

MCU Port P4 Usage

MCU, D420 port 4 is used for baseband control.

Port Pin	MCU pin	Control Function	Remark
P40	5	SLIC–CTRL 0	
P41	6	SLIC–CTRL 1	
P42	7	SLIC–CTRL 2	
P43	8	RS_DSR	
P44	9	EEPROM SCK	
P45	10	EEPROM SDA	
P46	11	EEPROM write enable	Active low
P47	12	RS_CTS	

Baseband A/D Converter Channels usage in N450 and D420

The auxiliary A/D converter channels inside RFI2 N450 are used only for measuring of the system board temperature by the MCU.

The MCU has 4 10 bit A/D channels which are used for baseband voltage monitoring. The MCU can measure supply voltage, accessory detection (ID), loop current (IBBDET) and output voltage of the line adapter power supply unit (VBBDET) by using it‘s own converters.

Baseband N450 A/D Converter Channel Usage

Name:	Usage:	Input volt. range
Chan 0	System board temperature	0...3.2 V
Chan 1–7	not used	

MCU Baseband A/D Converter Channel Usage

Name:	Usage:	Input volt. range
Chan 0	Supply voltage	0...3.2 V
Chan 1	Accessory detection	0...3.2 V
Chan 2	IBBDET	0...3.2 V
Chan 3	VBBDET	0...3.2 V

Supply Voltage Measurement

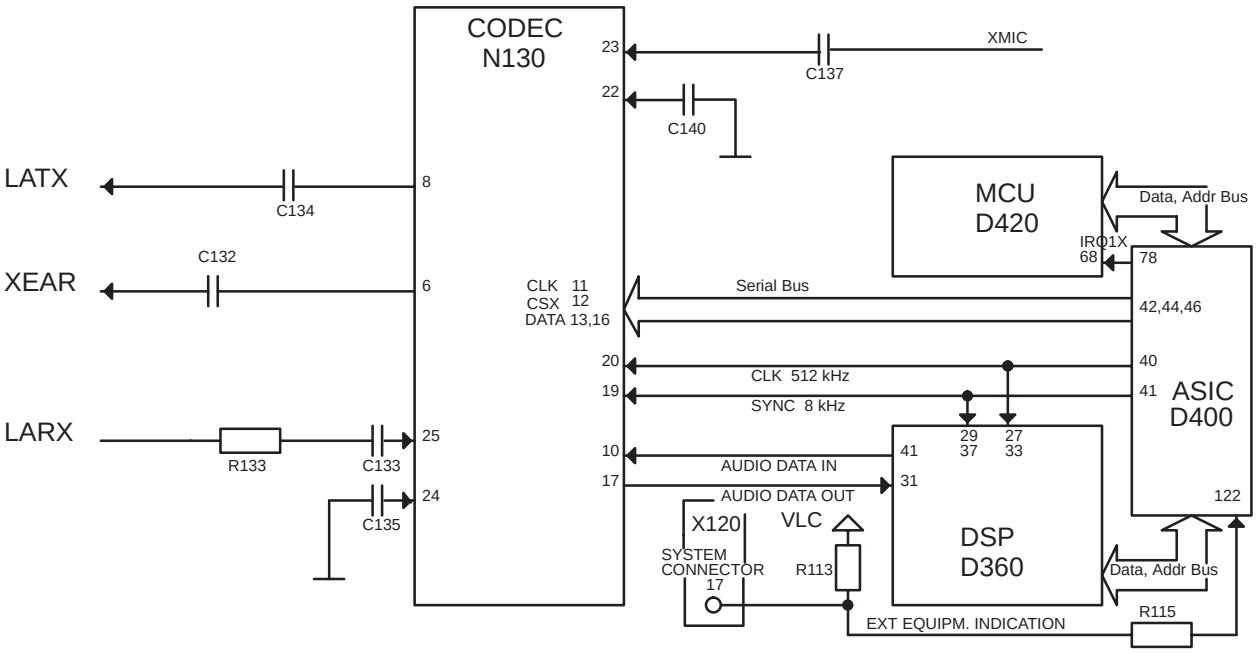
The supply voltage is measured using MCU N420 A/D converter channel 0. The supply voltage supplied to the A/D converter input is switched off when the baseband is powered off. The supply voltage measurement voltage is supplied by PSCLD N300, which performs switch–off, and scaling with a scaling factor of R1(R1+R2). The measurement voltage is filtered by a capacitor to achieve an average value that is not depending upon the current consumption behavior of the baseband. To be able to measure the supply voltage during transmission pulse, the time constant must be short. The value for the filtering capacitor is set to 10 uF C316. The scaling factor used to scale the supply voltage must be 1:3, which means that a 9V supply voltage will give 3V A/D converter input voltage. The A/D converter value in decimal can be calculated using the following formula:

$A/D = 1023xR1xU_{BAT}/((R1+R2)xU_{ref}) = 1023xU_{BAT}xK$

where K is the scaling factor. $K = R1/((R1+R2)xU_{ref)}$.

Audio Control

The audio codec N130 is controlled by the MCU D420. The ASIC generates a 512 kHz data clock, and a 8 kHz synchronization signal for the PCM data bus. Data is put out on the bus at the rising edge of the clock and read in at the falling edge. Data from the DSP D360 to the audio codec N130 is transmitted as a separate signal from data transmitted from the audio codec, N130 to the DSP D360. The communication is full duplex synchronous. The transmission is started at the falling edge of the synchronization pulse. 16 bits of data is transmitted after each synchronization pulse.



The 512 kHz clock is generated from 13 MHz using a PLL type of approach, which means that the output frequency varies as the PLL adjusts the frequency. The average frequency is 512 kHz. The clock is not supplied to the codec when it is not needed. The clock is controlled by both MCU and DSP. DTMF tones are generated by the audio codec and for that purpose, the 512 kHz clock is needed. The MCU must switch on the clock before the DTMF generation control data is transmitted on the serial control bus.

The serial control bus uses clock, data, and chip select to address the device on the bus. This interface is built into the ASIC, and the MCU writes the destination and data to the ASIC registers. The serial communication is then initiated by the ASIC. Data can be read form the audio codec N130 via this bus.

DSP

The DSP used in TFE–1 model C is the TI 320LC546. This is a 16 bit DSP that can use external and/or internal memory access. The DSP can operate in two modes microprocessor mode or micro–controller mode. The difference between the two modes is that in microprocessor mode the DSP boots from external memory, while in the micro–controller mode the DSP boots from internal ROM. The DSP external memory access is divided into data, program, and I/O access. The type of access is indicated on three control pins that can be used for memory control.

The DSP D360 executes code from the internal ROM. The baseband also provides external memories for the DSP, D371, D372, D381, and D382 (Note: These memories are not fitted in all transceivers). The DSP is capable of addressing 64 kword of memory. The memory area is divided into a code execution area and a data storage area. The code execution area is located at address 4000H–FFFFH in the internal ROM. The external memories are arranged in such a way that the DSP can access the external memories both as data storage and code execution. The memory chip select is taken from the memory access strobe signal from the DSP. This means that the memory is active during any memory access. The SRAMs are configured in chip select controlled write mode. This means that both the write signal and the output enable signal are active at the same time, and the actual write occurs at the rising edge of the chip select signal. This implementation is required since the DSP supports only one signal for write/read control.

The DSP is operating from the 13 MHz clock. In order to get the required performance, the frequency is internally increased by a PLL by a factor of 3. The PLL requires a settling time of 50 us after that the clock has been supplied before proper operation is established. This settling counter is inside the DSP although the ASIC D400 contains a counter that will delay the interrupt with a programmable amount of clock cycles before the interrupt causing the clock to be switched on is presented to the DSP. The DSP has full control over the clock supplied to it. When the DSP is to enter the sleep mode the clock is switched off by setting a bit in the ASIC register. The clock is automatically switched on when an interrupt is generated.

The DSP also has two synchronous serial channels for communication. One channel is used for data transmission between the DSP and the audio codec. This channel is operating at 512 kbits, and clock and synchronization signal is provided by the ASIC D400. The other channel is used for debugging purposes, and uses the same clock and synchronization signals. The DSP has an interrupt controller servicing four interrupts and one non maskable interrupt, NMI. The interrupts have fixed priority which can only be changed by changing the interconnection between the interrupt sources by HW.

The ASIC contains DSP support functions as modulator, encryption/decryption using algorithms A5/A51, RF power ramp generation/AGC control, AFC control, synthesizer serial interface, frame counters, timer, RFI2 interface, and RX and TX power control timing. The RF power ramp timing/AGC control, AFC control,

and synthesizer control are timed to the value of the frame counter. This means that data is loaded into the registers, and transferred when the frame counter and the reference values match. This allows timing of the synthesizer control power ramp and start of TX data to be controlled very precisely.

As the receiver and the transmitter is not operating at the same time, the TX power ramp function is used to control the AGC in the receiver during the reception. This requires the DSP to continuously modify the values in the TX ramp SRAM to fit the ramp during TX and the AGC value during reception.

DSP ASIC Access

The DSP is accessing the ASIC in the DSP I/O area. 2 wait states are required for the ASIC access. Some of the DSP registers located in the ASIC are retimed to the internal ASIC clock and requires special handling with respect to consecutive writing. This means that the same register can not be written again until a specified time has passed. To cope with this, DSP is inserting NOP instructions to satisfy this requirement.

DSP Interrupts

The DSP supports 4 external interrupts. Three interrupts are used. The ASIC, D400 generates two of the interrupts. One interrupt is generated by the RFI2 N450 auxiliary A/D converter. This interrupt is generated when a baseband measurement A/D conversion is completed. The interrupts to the DSP are active low.

INT0, which is the highest priority interrupt, is used for data reception from the receiver and is generated by the ASIC. The INT1 signal is used for auxiliary A/D channel conversions generated by the RFI2. This interrupt is generated by RFI2 and is a result of measurement requests from the DSP. INT3 is a low priority interrupt generated by the ASIC timer. The DSP programs the timer value and an interrupt is given when the timer expires. The interrupt must be active at least 1 DSP clock cycle as it is sampled on the rising/falling edge by the DSP. All interrupts are active low.

Unused interrupt controller inputs are tied high.

DSP Serial Communications Interface

The DSP contains two synchronous serial communications interfaces. One of the interfaces is used to communicate with the audio codec N130. The 512 kHz clock required for the data transfer is provided by D400 as well as the 8 kHz synchronization signal. Data is transferred on to lines, RX and TX creating a full duplex connection. Data is presented on the bus on the first rising edge of the clock after the falling edge of the synchronization pulse. Data is read in by each device on the falling edge of the clock. Data transfer is 16 bits after each synchronization pulse.

The DSP D360 has control over the clock provided to the audio codec. The DSP can switch on the clock to start the communication, and switch it off when it is not needed. This clock is also under control of MCU D420.

RF Synthesizer Control

The synthesizer control is performed by the DSP D360 using the ASIC D400 as the interfacing and timing device. Different synthesizer interfaces are supported, and the required interface can be selected by the DSP at the initialization stage of the ASIC. The synthesizer interface also includes timing registers for programming synthesizer data. The DSP loads the synthesizer data into the transmission registers in the ASIC synthesizer interface together with the timing information. The system timing information is used for synthesizer data loading. When the system timing register, frame counter, value matches the timing value programmed into the synthesizer interface, the interface transmits the loaded data to the RF synthesizer, and the VCO frequency is changed accordingly. As the synthesizer may be powered off when not needed, the interface pins towards the synthesizer can be put in tri–state or forced low when the interface is not active.

RFI2 N450 Operation

The RFI2 N450 contains the A/D and D/A converters to perform the A/D conversion from the received signal and the D/A converters to perform the conversion for the modulated signal to be supplied to the transmitter section. In addition, the RFI2 chip also contains the D/A converter for providing AFC voltage to the RF section. This AFC voltage controls the frequency of the 13 MHz VCXO which supplies the system clock to the baseband. The RFI2 N450 also contains the D/A converter to control the RF transmitter power control. The power control values are stored in the ASIC D400 and at the start of each transmission, the values are read from the ASIC D400 to the D/A converter producing the power control pulse. This D/A converter is used during the reception to provide AGC for the receiver RF parts.

The RFI2 contains the interface between the baseband and the RF. The RFI2 circuit contains the A/D converters required for the receiver and the D/A converters required for the transmission. In addition, the RFI2 contains a 10 bit D/A converter for AFC control, and one of the receiver A/D converters has a multiplexed input for 8 additional channels used for baseband monitoring functions. The A/D converters are 12 bit sigma delta type. This means that the digital output is centered around the reference voltage and the output value is both negative and positive. The RFI2 has an internal reference voltage for the A/D and D/A converters that can be switched off to save power. The reference has external filtering capacitors to improve the converter performance. The transmitter D/A converters are followed by interpolator and post filter. The filter is of switch capacitor type and the filter parameters are taken into account when modulator parameters are calculated. The AFC D/A converter is static and requires no

clock for operation. This means that the RFI2 clock can be switched off and the AFC value will be kept.

One of the A/D converters used for receiver signal conversion can be used as an auxiliary converter that supplies 8 channels for baseband measurement purposes. When the converter is used in this mode, each conversion generates an interrupt directly to the DSP. The DSP operates this converter via the ASIC D400.

Data communication between the ASIC D400 and RFI2 N450 is carried out on a 12 bit parallel data bus. The ASIC D400 uses 4 address lines to access RFI2 N450. Depending on the direction of the communication, either the write control signal is used to write data to RFI2 N450 or the read signal is used to read data from RFI2 N450. The ASIC D400 supplies 13 MHz clock to the RFI2 N450. This clock is used as reference for the A/D and D/A converters. Communication between the ASIC D400 and the RFI2 N450 is related to the clock.

The auxiliary channels supported by the RFI2 uses one of the receiver A/D converters as the A/D converter. Due to the type of converter used for the receiver converters, the value read from the auxiliary channels can be negative. The input voltage applied to the auxiliary channels must be within 0.5–3.0 V. A 12 bit value is received from the auxiliary channel measurement. The auxiliary channel conversion complete is sent direct to the DSP as an interrupt, INT1. The DSP reads the value using direct access through the ASIC to the RFI2 converter. The conversion is started by the DSP writing the address of the channel to be measured to the ASIC register. The ASIC then writes the selected channel to RFI2, and the conversion is started. The DSP may sample the same channel for more than one value as the A/D converter will produce continuously new values. Several samples may be used for example in supply voltage measurement to calculate an average value from the results.

The RFI2 N450 digital supply is taken from the baseband main digital supply. The analog power supply, 4.5V is generated by a regulator supplied from the RF section. The analog power supply is always supplied as long as the baseband is powered, if R311 is assembled. The RFI2 N450 analog power supply can be switched off during sleep by removing R311 and adding R312. In this case the RFI2 N450 analog power supply is in the control of the PSCLD N300 sleep control signal.

Receiver Timing and AGC

RF receiver power on timing is performed by the ASIC D400. The DSP D360, can program the time when the receiver is to be powered on. The timing information is taken from the system timing that is based upon the frame counter inside the ASIC D400, which is synchronized to the base station carrier frequency using AFC to tune the receiver. As transmission and reception takes place at different times, the D/A converter used for transmitter power control is used to control the AGC of the receiver during reception. This requires the DSP D360 to alter the content of the SRAM containing the information that is written to the D/A converter for the reception and the transmission.

RF Transmitter Timing and Power Control

The RF Power Amplifier (PA) timing control is performed by the ASIC D400. The power control is performed by the ASIC D151 using the D/A converter in N450. The ASIC D400 controls the power supply voltage to the RF transmitter sections. As the first step, the relevant circuits are powered on using the TX power control output from the ASIC D400. The timing for powering on the TX circuits is generated from the ASIC internal system timing circuitry, frame counter. As the RF TX circuits need time to stabilize after power on before the actual transmitter can be started, there is a programmable delay before the ASIC D400 starts to write the power ramp data to the D/A converter inside N450. The TXC signal which is generated in this way controls the power ramp of the PA and the power level for that burst. At the end of the burst the power ramp is written to the D/A converter inside N450. The data that creates the power ramp and final power level is stored in a SRAM inside the ASIC D400. At the start of the ramp, the contents of the SRAM are read out in increasing address order. At the end of the ramp the contents are read out in decreasing address order. The power level during the burst is determined by the last value in the SRAM, this value is the value that will remain in the D/A converter during the burst. The DSP D360 may change the shape of the falling slope of the power ramp by writing new values to the power ramp SRAM during the burst.

As the transmitter may have to adjust the transmitter burst due to the distance from the base station there is an additional timer for this purpose. This timing is called the timing advance and will cause the transmission to start earlier when the distance to the base station increases.

SIM Interface

The SIM interface is the serial interface between the smart card and the baseband. The SIM interface logic levels are 5V, since no 3V technology SIM is yet available. The baseband is designed in such a way that a 3V technology SIM can be used whenever it is available. The SIM interface signals are generated inside the ASIC. The signals coming from the ASIC are converted to 5V levels. The PSCLD circuit is used as the logic voltage conversion circuit for the SIM interface. The PSCLD circuit also contains the voltage regulator for the SIM power supply. The control signals from the ASIC to PSCLD are at 3V level and the signals between PSCLD and the SIM are 5V levels. An additional control line between the ASIC and the PSCLD is used to control the direction of the DATA buffer between the SIM and the PSCLD. In a 3V technology environment this signal is internal to the ASIC only. The pull up resistor required on the SIM DATA line is integrated into the PSCLD, and the pull–up is connected to the SIM regulator output inside PSCLD. In idle, the DATA line is kept as input by both the SIM and the interface on the baseband. The pull–up resistor is keeping the DATA line in it’s high state.

The power up and power down sequences of the SIM interface are performed according to ISO 7816–3. To protect the card from damage when the power supply is removed during power on, there is a control signal, CARDIN, that au-

tomatically starts the power down sequence. The CARDIN information is taken from 5 V regulator N350.

Since the power supply to the SIM is derived from PSCLD also using 3V technology SIM, the power supply voltage of the SIM regulator is programmable 3.15/4.8 V. The voltage is selected by using the serial control bus to PSCLD. The default value is set to 3.2V nominal.

For cross compatibility reasons, the interface should always be started up using 5V. The 3V technology SIM will operate at 5V but a 5V SIM will not operate at 3V. The supply voltage is switched to 3V if the SIM can accept that. The SIM has a bit set in a data field indicating it's capability of 3V operation.

The regulator control signal is derived from the ASIC, and this signal controls the operation of the SIM power supply regulator inside PSCLD. To ensure that the powered off ASIC doesn't cause any uncontrolled operations at the SIM interface, the PSCLD signals to the SIM are forced low when the PURX signal is active low. This implementation will ensure that the SIM interface can not be activated by any external signal when PSCLD has PURX active. When PURX goes inactive the control of the interface signals are given back to the ASIC signals controlling PSCLD SIM interface operations.

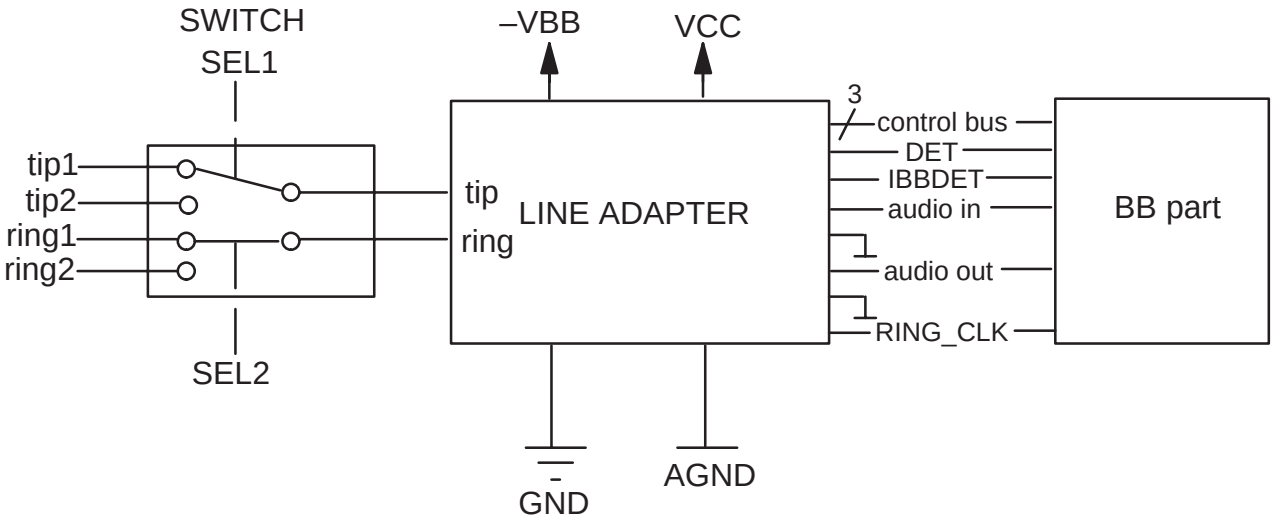
The clock to the SIM can be switched off if the SIM card allows stopping of the clock. The clock can be stopped either in high or low state, determined by the card data. For cards not allowing the clock to be stopped there is a 1.083 MHz clock frequency that can be used to reduce the power consumption while the clock is running. In this case the VCO must be running all the time. When the clock is stopped, and the status of the CARDIN signal changes, power is switched OFF, the clock to the SIM is restarted inside the ASIC, and the SIM power down sequence is performed.

To be able to handle current spikes as specified in the SIM interface specifications, the SIM regulator output from PSCLD must have a ceramic capacitor of 100 nF connected between the output and ground close to the SIM interface connector. To be able to cope with the fall time requirements and the disconnected contact measurements in type approval, the regulator output must be actively pulled down when the regulator is switched off. This active pull–down must work as long as the external battery is connected and the battery voltage is above the PSCLD reset level.

The SIM power on procedure is controlled by the MCU. The MCU can power up the SIM only if the CARDIN signal is in the inactive state low. Once the power up procedure has been started, the ASIC takes care that the power up procedure is performed according to ISO 7816–3.

The SIM interface uses two clock frequencies 3.25 MHz or 1.625 MHz during SIM communication. The data transfer speed in the SIM GSM session is specified to be the supplied clock frequency/372. The ASIC SIM interface supplies all the required clock frequencies as well as the required clock frequency for the UART used in the SIM interface data transmission/reception.

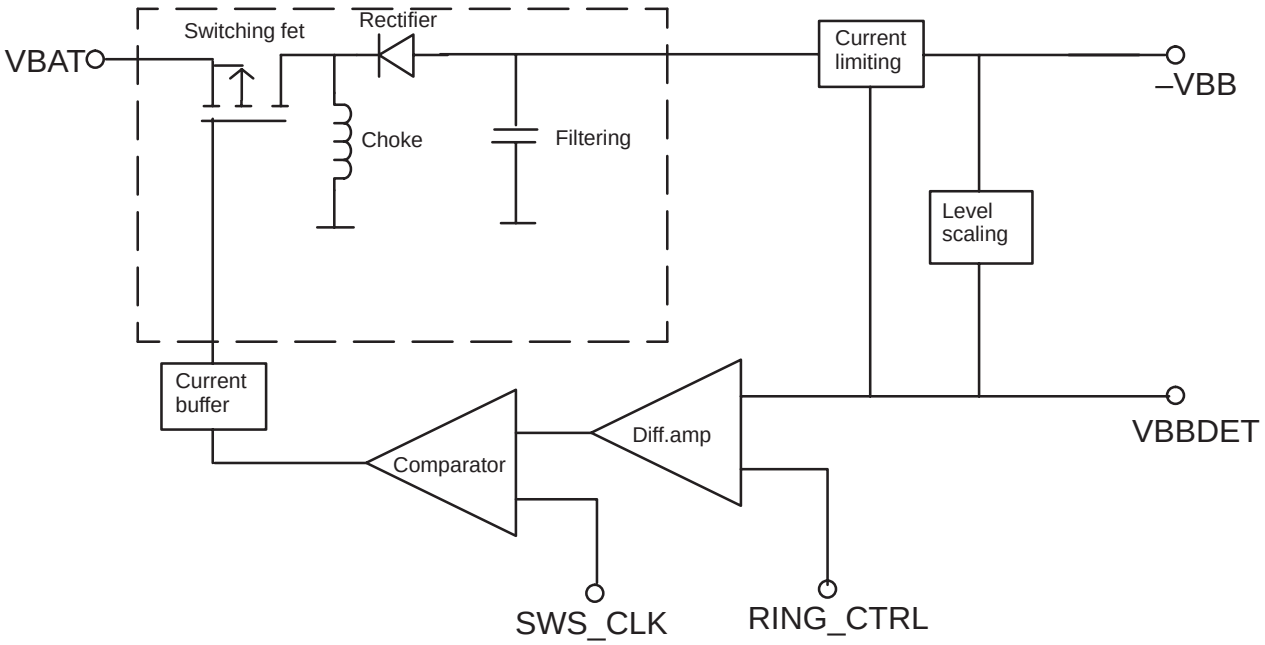
Line Adapter



The Line Adapter makes 2 to 4–wire transformation between the termination and the base part of the terminal. The 2–wire interface is of balanced line type, and the voltage between tip and ring lines is about 40 V. The 4–wire part is a normal audio–input (LATX) and audio–output (LARX) interface. The line Adapter is based on an Am79R79 SLIC circuit. It is controlled by the MCU with a 3 V parallel bus (3 bits). SLIC uses three different states: ringing, active, and standby. The MCU can detect the termination state (ON–HOOK/OFF–HOOK) by the DET pin. Ringing and metering are done via the RING_CLK line. In ringing state, the MCU feeds 25 Hz to RINGIN pin. The circuit operates with two different operating voltages: VCC (+ 5 V) and –VBB (– 50 V or – 60 V), and with two grounds GND and AGND. Loop current, Hook threshold, and ring waveform are set by discrete components connected to circuits pins RDC, RD, and RINGIN. Loop current can be detected with the IBBDET line, which is connected to BB part.

The 2–wire line is divided to two separate 2 wire lines, tip1–ring1 (telephone), and tip2–ring2 (fax machine). The divider is implemented with fet switches, and both lines can be switched on or off separately. Control is made by the MCU with SEL1 and SEL2 lines. Both 2 wire lines are protected by transient voltage suppressors (82 V) connected from each line to ground.

Line Adapter Power Supply



The Line Adapter power supply unit is of inverting switch mode power supply type with PWM control. Voltage and current limitation are implemented in the feedback. The main clock signal SWS_CLK is made by MCU, and it is 125 kHz square wave. With RING_CNTR line output voltage can be increased from – 50 V to – 60 V when SLIC is in ringing state. The VBBDET line is used to detect output voltage level. Current limitation is set to about 50 mA.

RF Block

Introduction

The RF module carries out all the RF functions of the transceiver. This module works in the GSM system.

Components are located on one side of the PCB.

EMC leakage is prevented with metallized shield A on side one, and metallized shield B on side two. Both shields also conduct heat out of the inner parts of the phone, thus preventing excessive temperature rise.

Receiver

The receiver system is based on double conversions. There is also space diversity in this receiver. Space diversity is created by using two separate RX antennas and partially separated signal routes.

The received RF signal from the antenna is fed via a duplex filter or receiver filter to the receiver unit. The signal is amplified by a discrete low noise preamplifier. The gain of the amplifier is controlled by the AGC control lines (ANT1SEL/ANT2SEL). The nominal gain of 21 dB is reduced about 36 dB. After the preamplifier the signal is filtered by SAW RF filter. The filter rejects spurious signals coming from the antenna and spurious emissions coming from the receiver unit.

The filtered RF signal is down converted by a passive diode mixer. The frequency of the first IF is 71 MHz in GSM. The first local signal is generated by the UHF synthesizer. The first IF signal is amplified and then it is filtered by SAW filter. The filter rejects adjacent channel signal, intermodulating signals and the last IF image signal.

The filtered IF signal is fed to the receiver part of the integrated RF circuit CRFRT. In CRFRT the filtered IF signal is amplified by an AGC amplifier which has gain control range of 57 dB. The gain is controlled by an analog signal via TXC–line.

The amplified IF signal is down converted to the last IF in the mixer of CRFRT. The last local signal is generated from VHF VCO by dividing the original signal by 4 in the dividers of CRFRT.

The last IF frequency is 13 MHz. The last IF is filtered by a ceramic filter. The filter rejects signals of the adjacent channels. The filtered last IF is fed back to CRFRT where it is amplified and fed out to RFI via RXINN and RXINP –lines.

Frequency Synthesizers

The stable frequency source for the synthesizers and base band circuits is a discrete voltage controlled crystal oscillator VCXO. The frequency of the oscillators is controlled by an AFC voltage, which is generated by the base band circuits.

The UHF PLL generates the down conversion signal for the receiver and the up conversion signal for the transmitter. The UHF VCO is a discrete oscillator. The working assumption for PLL circuit is Philips UMA1018.

The VHF PLL signal (divided by 4 in CRFRT) is used as a local for the last mixer. Also the VHF PLL signal (divided by 2 in CRFRT) is used in the I/Q modulator of the transmitter chain.

Transmitter

The TX intermediate frequency is modulated by an I/Q modulator contained on transmitter section of CRFRT IC. The TX I and Q signals are generated in the RFI interface circuit and they are fed differentially to the modulator.

Modulated intermediate signal is amplified or attenuated in temperature compensated controlled gain amplifier (TCGA). The output of the TCGA is amplified and the output level is typically –15dBm.

The output signal from CRFRT is band–pass filtered to reduce harmonics and the final TX signal is achieved by mixing the UHF VCO signal and the modulated TX intermediate signal with passive mixer. After mixing the TX signal is amplified and filtered by two amplifiers and one filter. This filter is dielectric filter. After these stages the level of the signal is typically 0.65 mW (–2 dBm).

The discrete power amplifier amplifies the TX signal to the desired power level. The maximum output level is typically 2.0 W.

The power control loop controls the output level of the power amplifier. The power detector consists of a directional coupler and a diode rectifier. Transmitted power is controlled with controlled gain amplifier (TCGA) on TX–path of CRFRT. Power is controlled with TXC and TXP signals. The power control signal (TXC), which has a raised cosine form, comes from the RF interface circuit, RFI.

RF Characteristics

Receiver

ITEM	GSM
RX frequency range , MHz	935...960
Type	2 IFs linear
Intermediate frequencies , MHz	71, 13
3 dB bandwidth ,kHz	+/– 100
Reference noise bandwidth ,kHz	270
Sensitivity , dBm	–104 S/N ratio > 8 dB BN=135 kHz
AGC dynamic range dB	93 typ.
Receiver gain ,dB	83 typ.
RF front end gain control range,dB	36
2nd IF gain control range, dB	57
Input dynamic range ,dBm	–104 ... –10
Gain relative accuracy in receiving band dB	+/– 1.5
Gain relative accuracy on channel ,dB	+/– 0.4

Pre–filters

The duplex filter consists of two functional parts; RX and TX filters. The TX filter rejects the noise power in the RX frequency band and TX harmonic signals. The RX filter rejects blocking and spurious signals coming from the antenna.

For diversity use, there is a separate RX filter, which rejects blocking and spurious signals coming from antenna 2.

Pre–amplifier

The bipolar pre–amplifier amplifies the received signal coming from the antenna. In the strong field conditions the gain of the amplifier is reduced 36 dB typically.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Frequency band	935–960			MHz
Supply voltage	4.275	4.5	4.725	V
Current consumption	10	12	14	mA
Insertion gain	19	21	22	dB
Gain flatness		+/– 0.5		dB
Noise figure		1.2	1.5	dB
Reverse isolation	15			dB
Gain reduction	33	36	39	dB
IIP3	–6	–3		dBm
Input VSWR (Zo=50 ohms)			2.0	
Output VSWR (Zo=50 ohms)			2.0	

RX Interstage Filter

The RX interstage filter is a SAW filter. The filter rejects spurious and blocking signals coming from the antenna. It rejects the local oscillator signal leakage.

First mixer

The first mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer down converts the received RF signal to IF signal.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
RX frequency range	935		960	MHz
LO frequency range	1006		1031	MHz
IF frequency		71		MHz
Conversion loss	5	6	7	dB
IIP3	4	6		dBm
LO–RF isolation	15			dB
LO power level	–5	–3		dBm

First IF amplifier

The first IF amplifier is a bipolar transistor amplifier.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Operation frequency		71		MHz
Supply voltage	4.275	4.5	4.725	V
Current consumption		32	35	mA
Insertion gain	18	20	22	dB
Noise figure		3.0	4.0	dB
IIP3	3	5		dBm
Input impedance				matched to the mixer
Output impedance				matched to the filter

First IF filter

The first IF filter is a SAW filter. The IF filter rejects some spurious and blocking signals coming from the front end of the receiver. The IF filter makes the part of the channel selectivity of the receiver. It rejects adjacent channel signals (except the 2nd adjacent).

Receiver IF Circuit, RX part of CRFRT

The receiver part of CRFRT consists of an AGC amplifier of 57 dB gain, a mixer and a buffer amplifier for the last IF. The mixer of the circuit down converts the received signal to the last IF frequency. After external filtering the signal is amplified and fed to baseband circuitry. The supply current can be switched OFF by an internal switch, when the RX is OFF.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	4.275	4.5	4.725	V
Current consumption		32	44	mA
Input frequency range	45		87	MHz
Local frequency range of mixer	170		400	MHz
2nd IF range	2		17	MHz
Voltage gain of AGC amplifier	47			dB
Noise figure			16	Max gain
AGC gain control slope	40	84	100	dB/V
Mixer output 1dB compression point		1.0		Vpp
Gain of the last IF buffer		30		dB
Max output level after last IF buffer		1.6		Vpp

Last IF Filter

The last IF is 13 MHz. The ceramic filter on the last IF provides part of the channel selectivity of the receiver.

Transmitter

Item	GSM
TX frequency range	890...915 MHz
Type	Upconversion
Intermediate frequency	116 MHz
Maximum output power	2 W (33 dBm)
Gain control range	20 dB
Maximum RMS phase error	5 deg.

Modulator Circuit TX, part of CRFRT

The modulator is a quadrature modulator contained in Tx–section of CRFRT IC. The I– and Q– inputs generated by RFI interface are DC–coupled and fed via buffers to the modulator. The local signal is divided by two to get accurate 90 degrees phase shifted signals to the I/Q mixers. After mixing the signals are combined and amplified with temperature compensated controlled gain amplifier (TCGA). Gain is controlled with power control signal (TXC). The output of the TCGA is amplified and the maximum output level is typically –10 dBm.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	4.275	4.5	4.725	V
Supply current		35	45	mA
Transmit Frequency Input	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
LO input frequency	170		400	MHz
LO input power level		0.2		Vpp
LO input resistance	70	100	130	ohm
LO input capacitance		4		pF
Modulator Inputs (I/Q)	**Minimum**	**Typical / Nominal**	**Maximum**	**Unit / Notes**
Input bias current (balanced)			100	nA
Input common mode voltage	2.05	2.2	2.4	V
Input level (balanced)			1.1	Vpp
Input frequency range	0		300	kHz
Input resistance (balanced)	200			kohms
Input capacitance (balanced)			4	pF

Modulator Output	Minimum	Typical / Nominal	Maximum	Unit / Notes
Output frequency	85		200	MHz
Available linear RF power		–10		dBm, ZiL=50 ohms
Available saturated RF power		0		dBm, ZiL=50 ohms
Total gain control range	45			dB
Gain control slope		84		dB/V
Suppression of 3rd order prods	35			dB
Carrier suppression		35		dB
Single sideband suppression				dB

Modulator Output	Minimum	Typical / Nominal	Maximum	Unit / Notes
Noise floor			–135	dBm/Hz avg.
Transmitted I/Q phase balance drift in whole temperature range	–5 –2		5 2	deg
Transmitted I/Q amplitude balance drift in whole temperature range	 –0.5 –0.2		 0.5 0.2	dB

Up–conversion Mixer

The upconversion mixer is a single balanced passive diode mixer. The local signal is balanced by a printed circuit transformer. The mixer up–converts the modulated IF signal coming from quadrature modulator to RF signal.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
TX frequency range	890		915	MHz
LO frequency range	1006		1031	MHz
IF frequency		116		MHz
Conversion loss	6.0	7.0	8.0	dB
IIP3	0.0			dBm
LO – RF isolation	15.0			dB
LO power level	–5.0	–3.0	0.0	dBm

1st TX Buffer

The TX buffer is a bipolar transistor amplifier. It amplifies the TX signal coming from the upconversion mixer.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Operating freq. range	890		915	MHz
Supply voltage	4.275	4.5	4.725	V
Current consumption		4.5	5.0	mA
Insertion gain	8.0	9.0	10.0	dB
Input VSWR (Zo=50 ohms)			2.0	matched to the mixer
Output VSWR (Zo=50 ohms)			2.0	

TX interstage filters

The TX filters reject the spurious signals generated in the upconversion mixer. They reject the local, image and IF signal leakage and RX band noise, too.

2nd TX Buffer

The TX buffer is a bipolar transistor amplifier. It amplifies the TX signal coming from the first interstage filter.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Operating freq. range	890		915	MHz
Supply voltage	4.275	4.5	4.725	V
Current consumption	14	15	16	mA
Insertion gain	12.0	13.0	14.0	dB
Input VSWR (Zo=50 ohms)			2.0	
Output VSWR (Zo=50 ohms)			2.0	

Power Amplifier

The power amplifier is a three stage discrete amplifier. It amplifies the –2 dBm TX signal to the desired 33 dBmoutput level. It has been specified for 6.8 volts operation.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
DC supply voltage (no RF)			10	V
DC supply voltage (normal)	5.5	6.8	8.0	V
DC supply current	750		1290	mA
Operating freq range	890		915	MHz
Operating temp range			90	deg C
Output power	34.5	35.0	36.0	dBm normal cond
Output power	33.0	34.0	35.0	dBm extreme cond
Input power		–2.0		dBm
Gain	36.0	37.0	38.0	dB normal cond
Efficiency		42		% Po = 35 dBm
Input VSWR (Zo=50 ohms)			2.0	
Output VSWR (Zo=50 ohms)			2.0	
Harmonics: 2 fo 3 fo, 4 fo, 5 fo			–30 –40	dBc Po=35 dBm

Power Control Circuits

The power control loop consists of a power detector and a differential control circuit. The power detector is a combination of a directional coupler and a diode rectifier. The differential control circuit compares the detected voltage and the control voltage (TXC) and controls voltage controlled amplifier (in CRFRT) or the power amplifier. The control circuit is a part of CRFRT.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage using CRFRT	4.275	4.5	4.725	V
Supply current using CRFRT		3.0	5.0	mA
Power control range	20			dB
Power control inaccuracy			+/ – 1.0	dB
Dynamic range	80			dB
Input control volt range	0.2		3.0	V

Reference Oscillator

In GSM the reference oscillator is a discrete VCXO and the frequency is 13 MHz in product. The oscillator signal is used for a reference frequency of the synthesizers and the clock frequency for the base band circuits.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Center frequency		13		MHZ
Frequency tolerance	–18		18	ppm Vc=2.2 V
Frequency control range		67		ppm
Supply voltage	4.275	4.5	4.725	V
Current consumption		1.5	2	mA
Output voltage	1.3	1.7	2.0	Vpp sine wave for PLL
Harmonics			5	dBc
Control Voltage Range	0.3		3.7	V
Nominal Voltage (center freq)		2.0		V
Control Sensitivity	12	16	22	ppm/V
Frequency stability, vs. temperature vs. supply voltage vs. load vs. aging			 10 1 0.1 1	 ppm, –25...+70 deg.C ppm, 4.7 V +/– 5 % ppm, load +/– 10 % ppm, year
Operating temperature range	–20		70	deg. C
Load impedance: resistive part	2			kohm
parallel capacitance			20	pF

VHF PLL

The VHF PLL consists of the VHF VCO, PLL integrated circuit and loop filter. The output signal is used for the 2nd mixer of the receiver and for the I/Q modulator of the transmitter.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Start up settling time			5	ms
Phase error			1	deg. rms
Sidebands offset from carrier +/– 200 kHz +/– 400 kHz +/–1M Hz +/– 2 MHz +/– 3 MHz > 4 MHz		 –75 –84 <–85 <–85 <–85 <–85	 –70 –70 –70 –75 –85 –85	dBc

VHF VCO + Buffer

The VHF VCO uses a bipolar transistor as a active element and a combination of a chip coil and varactor diode as a resonance circuit. The buffer is combined into the VCO circuit so, that they use same collector current.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	4.275	4.5	4.725	V
Control voltage	0.5		4.0	V
Supply current		4.0	5.0	mA
Operation frequency		232		MHz
Output power level		168		mV_{rms} / 1 kohm
Control voltage sensitivity		12		MHz/V
Phase noise fo +/– 200 kHz fo +/– 1600 kHz fo +/– 3000kHz			 –123 –133 –143	dBc/Hz
Harmonics		–32	–30	dBc

UHF PLL

The UHF PLL consists of a UHF VCO, divider, PLL circuit and a loop filter. The output signal is used for the 1st mixer of the receiver and the upconversion mixer of the transmitter.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Start up settling time			5	ms
Phase error			4	deg. rms
Settling time +/– 93 MHz		525	800	us
Sidebands offset from carrier +/– 200 kHz +/– 400 kHz +/– 600 kHz > 1.0 MHz		 –80 –87 <–90 <–90	 –60 –65 –70 –80	dBc

UHF VCO + Buffer

The UHF VCO uses a bipolar transistor as a active element and a combination of a microstripline and a varactor diode as a resonance circuit.

UHF VCO Buffers

The UHF VCO output signal is divided into the 1st mixer of the receiver and the upconversion mixer of the transmitter. The UHF VCO signal is amplified after division. There is one buffer for TX and one for RX.

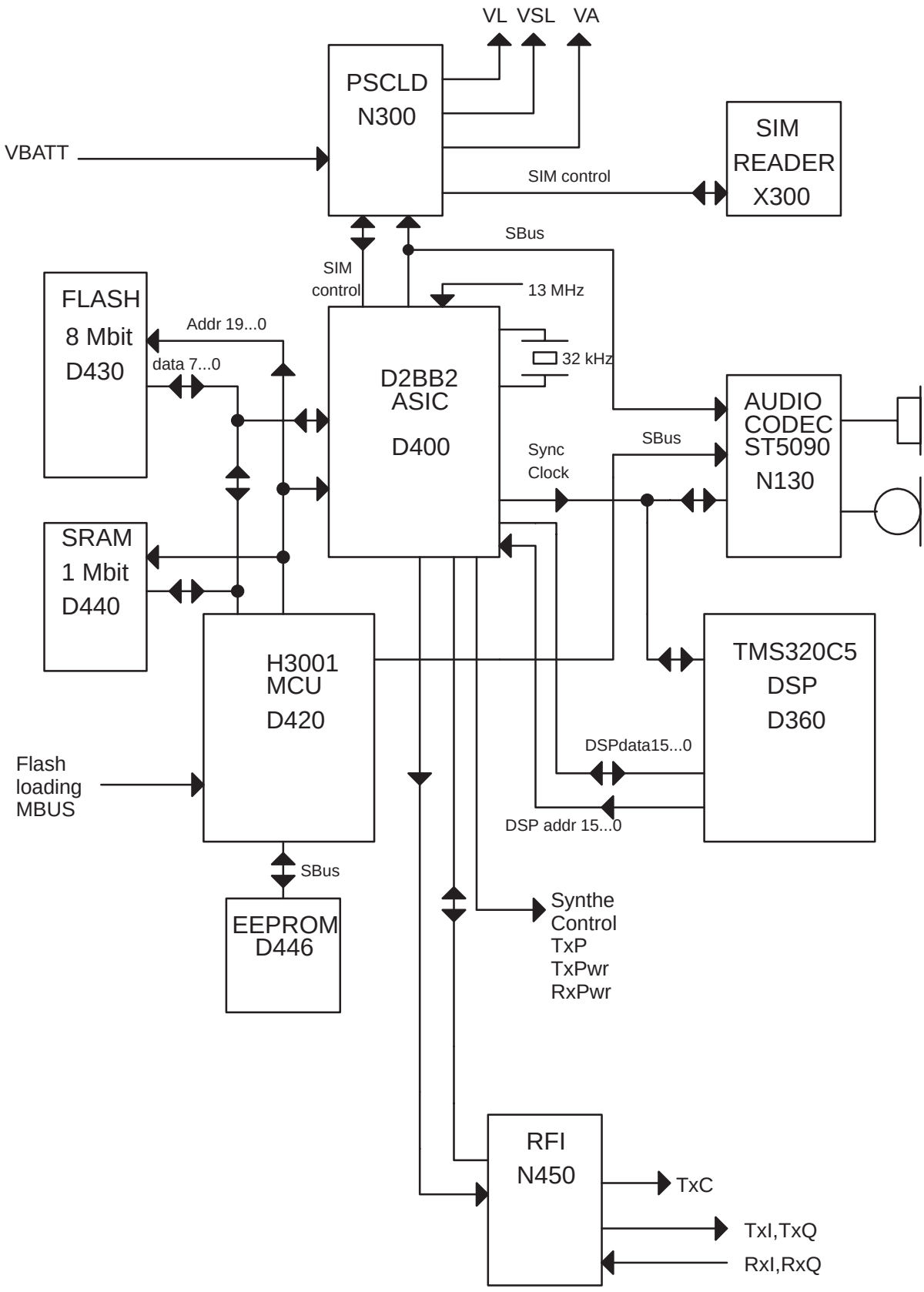
Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	4.275	4.5	4.725	V
Supply current	6	7	8	mA
Frequency range	see UHF VCO specification			MHz
Input power		–3		dBm
Harmonics			–10	dBc
Output amplitude		1000		mV_{rms} / 1 kohm

PLL Circuit

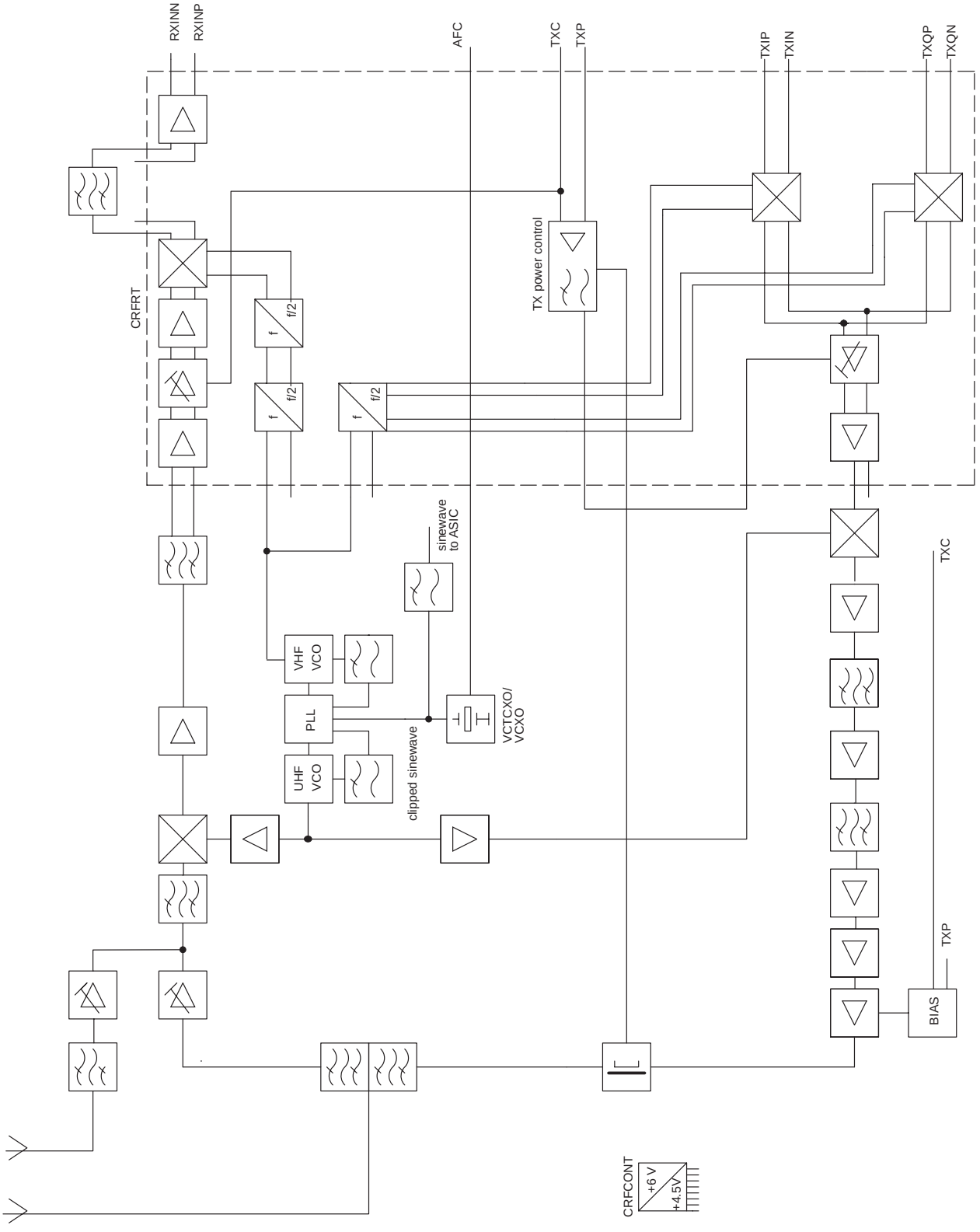
The PLL is PHILIPS UMA1018. The circuit is a dual frequency synthesizer including both the UHF and VHF synthesizers.

Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
Supply voltage	2.7		5.5	V
Supply current		10.0		mA
Principal input frequency	500		1200	MHz Vdd = 4.5 V
Auxiliary input frequency	20		300	MHz Vdd = 4.5 V
Input reference frequency	3		40	MHz, Vdd = 4.5 V
Input signal level	50 –10 –15 500		500 4 4	mV rms dBm main divider dBm aux. divider mVpp ref. divider

Interconnection Diagram of Baseband

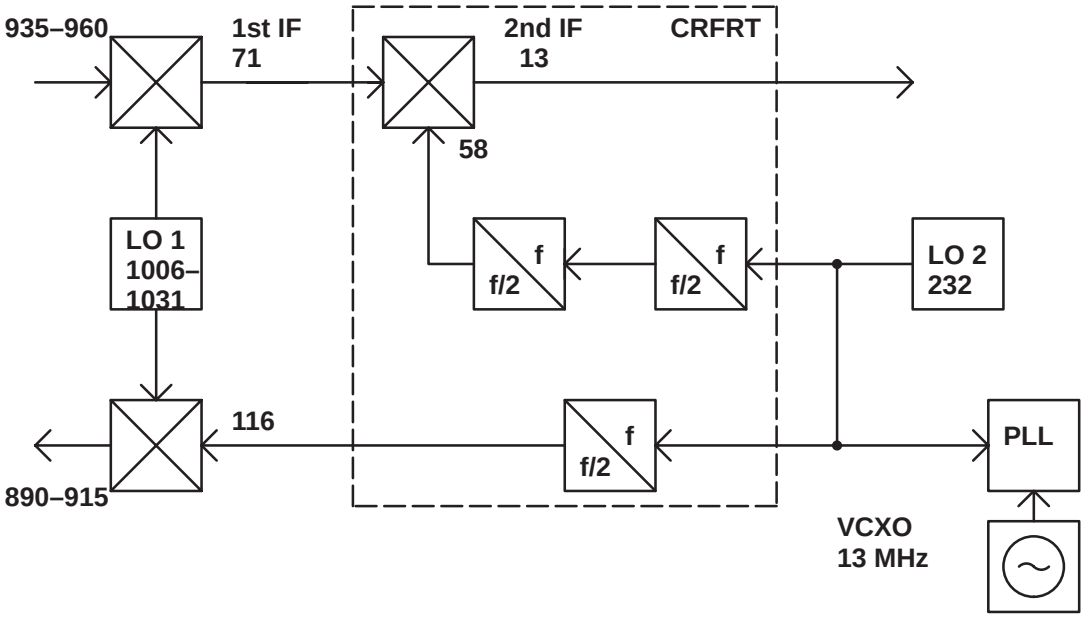


Block Diagram of RF

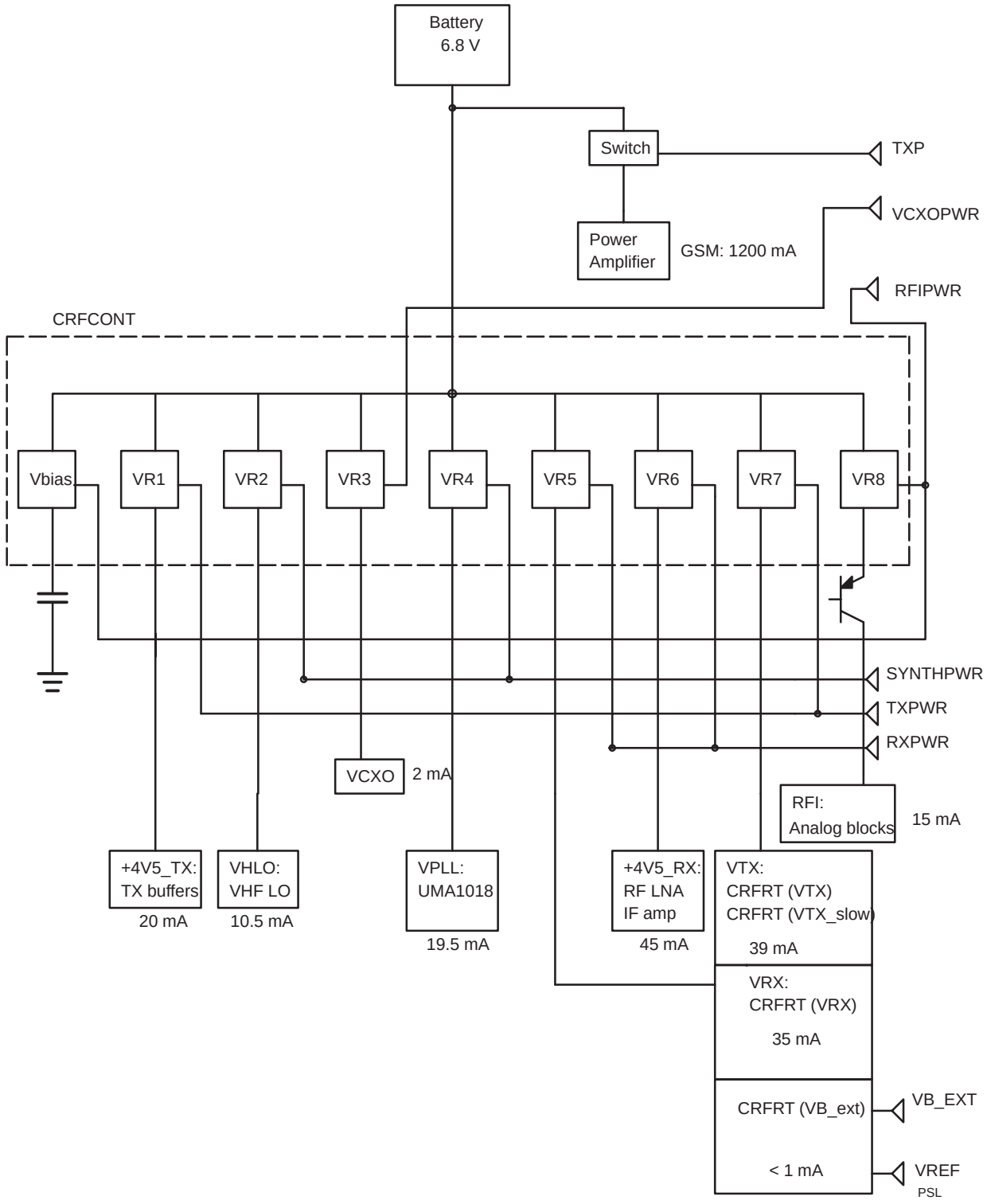


RF Frequency Plan

GSM



Power Distribution Diagram of RF



Immobilizer in TFE–1 model C

Introduction

Immobilizer is used to prevent the unauthorized moving of the terminal from its original location. If the terminal is moved it cannot anymore be used before the immobilizer is disabled by service personnel. The movement of the terminal can be detected by a push–button switch, which is located in the back cover of the terminal. When the terminal is installed in its desired location, the switch is pressed down towards the wall. Also the immobilizer function in the software is activated by the service personnel installing the terminal. After that, whenever the switch is opened e.g when the terminal is removed from the wall, it could be detected by the software and the terminal goes to a state, where only emergency calls are possible.

Immobilizer hardware

The hardware part of the Immobilizer is implemented around the baseband ASIC, (D400). The main parts are a 74HC00 logic circuit (D410, quad NAND), which is used as a flip–flop, a back–up battery (G410) and a push–button switch (S410). The whole circuitry is described in the following section.

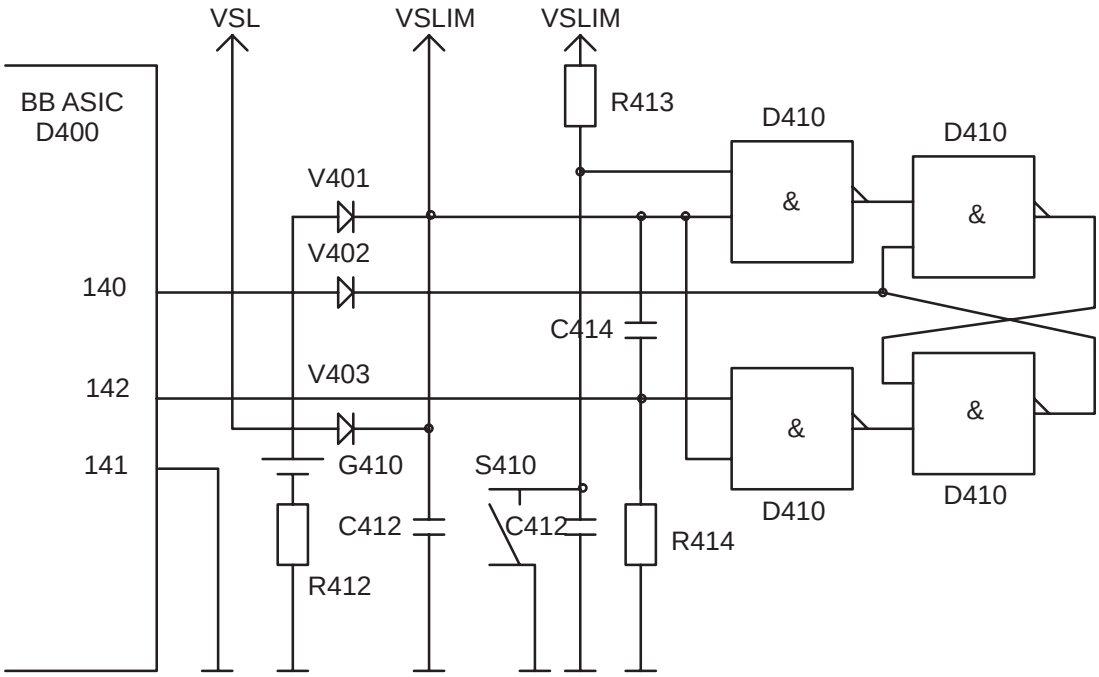


Figure 1.

The immobilizer uses three I/O pins of BART ASIC (D400). Pin 142 is used for writing to the immobilizer and from pin 140 the state of the flip–flop can be read. Pin 141 is connected to GND to indicate the presence of the immobilizer hardware.

When the immobilizer is activated, the state of the flip–flop is set by the switch and by the software via pin 142. After that, in the run–time, the state of the flip–flop is read every 4 seconds. As long as the terminal stays in its original location, the state is ”1”. When the terminal is moved, the switch (S410) opens and causes a state transition. After that the state of the flip–flop is found to be ”0” and the software sets the terminal to ”terminal moved” –state. In that state all the terminal LEDs are blinking and the message ”terminal moved” can be seen in the service handset.

The operating voltage of the immobilizer (VSLIM) is obtained from the 3.2 V logic supply (VSL). There is also a 130mAh lithium battery (G410), which is used as power supply in the situations when the terminal is not powered. This means, that the terminal can not be moved even if it has no power. In this case the flip–flop will change its state when the switch S410 is opened. When the terminal is powered again the movement will be detected.

Parts list of WT4C (EDMS Issue 3.5)

Code: 0201087

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R100	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R110	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R111	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R112	1430167	Chip resistor	47	5 % 0.063 W 0603
R113	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R114	1430167	Chip resistor	47	5 % 0.063 W 0603
R115	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R123	1430167	Chip resistor	47	5 % 0.063 W 0603
R124	1430167	Chip resistor	47	5 % 0.063 W 0603
R125	1430167	Chip resistor	47	5 % 0.063 W 0603
R126	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R127	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R128	1430001	Chip resistor	100	5 % 0.063 W 0603
R129	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R131	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R132	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R133	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R134	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R135	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R136	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R137	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R138	1430009	Chip resistor	220	5 % 0.063 W 0603
R141	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R142	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R143	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R146	1430159	Chip resistor	22	5 % 0.063 W 0603
R147	1430159	Chip resistor	22	5 % 0.063 W 0603
R148	1430055	Chip resistor	6.8 k	5 % 0.063 W 0603
R149	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R156	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R157	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R163	1430031	Chip resistor	100 k	1 % 0.063 W 0603
R164	1430031	Chip resistor	100 k	1 % 0.063 W 0603
R165	1430031	Chip resistor	100 k	1 % 0.063 W 0603
R168	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R169	1430294	Chip resistor	220 k	2 % 0.063 W 0603
R170	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R171	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R172	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R182	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R183	1430031	Chip resistor	100 k	1 % 0.063 W 0603
R184	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R185	1430087	Chip resistor	100 k	5 % 0.063 W 0603

R186	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R201	1430159	Chip resistor	22	5 % 0.063 W 0603
R202	1430159	Chip resistor	22	5 % 0.063 W 0603
R203	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R204	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R205	1430099	Chip resistor	330 k	5 % 0.063 W 0603
R206	1430099	Chip resistor	330 k	5 % 0.063 W 0603
R207	1430085	Chip resistor	82 k	5 % 0.063 W 0603
R208	1430085	Chip resistor	82 k	5 % 0.063 W 0603
R209	1430085	Chip resistor	82 k	5 % 0.063 W 0603
R210	1430085	Chip resistor	82 k	5 % 0.063 W 0603
R211	1430159	Chip resistor	22	5 % 0.063 W 0603
R212	1430159	Chip resistor	22	5 % 0.063 W 0603
R213	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R214	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R215	1430099	Chip resistor	330 k	5 % 0.063 W 0603
R216	1430099	Chip resistor	330 k	5 % 0.063 W 0603
R217	1430099	Chip resistor	330 k	5 % 0.063 W 0603
R219	1430099	Chip resistor	330 k	5 % 0.063 W 0603
R221	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R222	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R223	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R224	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R225	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R226	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R227	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R228	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R250	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R251	1430099	Chip resistor	330 k	5 % 0.063 W 0603
R252	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R253	1430031	Chip resistor	100 k	1 % 0.063 W 0603
R254	1430294	Chip resistor	220 k	2 % 0.063 W 0603
R256	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R257	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R260	1430085	Chip resistor	82 k	5 % 0.063 W 0603
R261	1430095	Chip resistor	220 k	5 % 0.063 W 0603
R262	1430085	Chip resistor	82 k	5 % 0.063 W 0603
R263	1430095	Chip resistor	220 k	5 % 0.063 W 0603
R264	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R265	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R266	1430075	Chip resistor	33 k	5 % 0.063 W 0603
R267	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R268	1430111	Chip resistor	1.0 M	5 % 0.063 W 0603
R269	1430111	Chip resistor	1.0 M	5 % 0.063 W 0603
R270	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R271	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R272	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R273	1430071	Chip resistor	22 k	5 % 0.063 W 0603

R274	1430075	Chip resistor	33 k	5 % 0.063 W 0603
R275	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R300	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R301	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R302	1430053	Chip resistor	5.6 k	5 % 0.063 W 0603
R311	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R313	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R331	1430001	Chip resistor	100	5 % 0.063 W 0603
R332	1430001	Chip resistor	100	5 % 0.063 W 0603
R344	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R346	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R361	1430167	Chip resistor	47	5 % 0.063 W 0603
R362	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R392	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R400	1430013	Chip resistor	330	5 % 0.063 W 0603
R403	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R407	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R408	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R409	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R410	1430073	Chip resistor	27 k	5 % 0.063 W 0603
R411	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R412	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R413	1430135	Chip resistor	10 M	5 % 0.063 W 0603
R414	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R420	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R421	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R436	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R437	1430167	Chip resistor	47	5 % 0.063 W 0603
R439	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R440	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R441	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R442	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R444	1430015	Chip resistor	470	5 % 0.063 W 0603
R445	1430015	Chip resistor	470	5 % 0.063 W 0603
R446	1430015	Chip resistor	470	5 % 0.063 W 0603
R447	1430015	Chip resistor	470	5 % 0.063 W 0603
R448	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R449	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R451	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R452	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R453	1430021	Chip resistor	680	5 % 0.063 W 0603
R454	1430021	Chip resistor	680	5 % 0.063 W 0603
R455	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R456	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R457	1800659	NTC resistor	47 k	10 % 0.12 W 0805
R460	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R461	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R501	1430151	Chip resistor	10	5 % 0.063 W 0603

R502	1430047	Chip resistor	3.3 k	5 % 0.063 W 0603
R503	1430047	Chip resistor	3.3 k	5 % 0.063 W 0603
R504	1430171	Chip resistor	68	5 % 0.063 W 0603
R505	1430055	Chip resistor	6.8 k	5 % 0.063 W 0603
R506	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R507	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R508	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R511	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R512	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R513	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R514	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R515	1430055	Chip resistor	6.8 k	5 % 0.063 W 0603
R518	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R519	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R520	1430001	Chip resistor	100	5 % 0.063 W 0603
R523	1430009	Chip resistor	220	5 % 0.063 W 0603
R524	1430159	Chip resistor	22	5 % 0.063 W 0603
R525	1430009	Chip resistor	220	5 % 0.063 W 0603
R526	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R527	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R528	1430013	Chip resistor	330	5 % 0.063 W 0603
R529	1430159	Chip resistor	22	5 % 0.063 W 0603
R541	1430159	Chip resistor	22	5 % 0.063 W 0603
R542	1430009	Chip resistor	220	5 % 0.063 W 0603
R543	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R544	1430039	Chip resistor	1.5 k	5 % 0.063 W 0603
R545	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R546	1430167	Chip resistor	47	5 % 0.063 W 0603
R547	1430015	Chip resistor	470	5 % 0.063 W 0603
R548	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R551	1430053	Chip resistor	5.6 k	5 % 0.063 W 0603
R552	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R553	1430053	Chip resistor	5.6 k	5 % 0.063 W 0603
R554	1430053	Chip resistor	5.6 k	5 % 0.063 W 0603
R555	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R556	1430053	Chip resistor	5.6 k	5 % 0.063 W 0603
R557	1430007	Chip resistor	180	5 % 0.063 W 0603
R558	1430007	Chip resistor	180	5 % 0.063 W 0603
R559	1430013	Chip resistor	330	5 % 0.063 W 0603
R560	1430047	Chip resistor	3.3 k	5 % 0.063 W 0603
R561	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R562	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R563	1430009	Chip resistor	220	5 % 0.063 W 0603
R566	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R568	1430009	Chip resistor	220	5 % 0.063 W 0603
R570	1430001	Chip resistor	100	5 % 0.063 W 0603
R571	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R572	1430079	Chip resistor	47 k	5 % 0.063 W 0603

R573	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R574	1430071	Chip resistor	22 k	5 % 0.063 W 0603
R576	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R578	1430077	Chip resistor	39 k	5 % 0.063 W 0603
R579	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R580	1430073	Chip resistor	27 k	5 % 0.063 W 0603
R601	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R602	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R603	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R701	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R702	1430173	Chip resistor	82	5 % 0.063 W 0603
R703	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R704	1430159	Chip resistor	22	5 % 0.063 W 0603
R705	1430013	Chip resistor	330	5 % 0.063 W 0603
R717	1430015	Chip resistor	470	5 % 0.063 W 0603
R721	1430151	Chip resistor	10	5 % 0.063 W 0603
R722	1430015	Chip resistor	470	5 % 0.063 W 0603
R723	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R725	1430039	Chip resistor	1.5 k	5 % 0.063 W 0603
R731	1430073	Chip resistor	27 k	5 % 0.063 W 0603
R732	1430001	Chip resistor	100	5 % 0.063 W 0603
R733	1430075	Chip resistor	33 k	5 % 0.063 W 0603
R734	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R736	1430159	Chip resistor	22	5 % 0.063 W 0603
R737	1430009	Chip resistor	220	5 % 0.063 W 0603
R738	1430009	Chip resistor	220	5 % 0.063 W 0603
R739	1430009	Chip resistor	220	5 % 0.063 W 0603
R746	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R748	1430009	Chip resistor	220	5 % 0.063 W 0603
R751	1412279	Chip resistor	2.2	5 % 0.1 W 0805
R752	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R761	1430021	Chip resistor	680	5 % 0.063 W 0603
R762	1430007	Chip resistor	180	5 % 0.063 W 0603
R763	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R764	1430023	Chip resistor	820	5 % 0.063 W 0603
R765	1430142	Chip resistor	4.7	5 % 0.063 W 0603
R773	1430019	Chip resistor	560	5 % 0.063 W 0603
R774	1430087	Chip resistor	100 k	5 % 0.063 W 0603
R776	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R777	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R779	1430151	Chip resistor	10	5 % 0.063 W 0603
R780	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R781	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R783	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R784	1430167	Chip resistor	47	5 % 0.063 W 0603
R785	1430013	Chip resistor	330	5 % 0.063 W 0603
R786	1430041	Chip resistor	1.8 k	5 % 0.063 W 0603
R793	1430069	Chip resistor	18 k	5 % 0.063 W 0603

R800	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R801	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R802	1430079	Chip resistor	47 k	5 % 0.063 W 0603
R803	1430001	Chip resistor	100	5 % 0.063 W 0603
R804	1430069	Chip resistor	18 k	5 % 0.063 W 0603
R805	1430069	Chip resistor	18 k	5 % 0.063 W 0603
R806	1430065	Chip resistor	10 k	5 % 0.063 W 0603
R807	1430041	Chip resistor	1.8 k	5 % 0.063 W 0603
R808	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R811	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R812	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R813	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R814	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R815	1430043	Chip resistor	2.2 k	5 % 0.063 W 0603
R816	1430081	Chip resistor	56 k	5 % 0.063 W 0603
R817	1430165	Chip resistor	39	5 % 0.063 W 0603
R818	1430035	Chip resistor	1.0 k	5 % 0.063 W 0603
R819	1430001	Chip resistor	100	5 % 0.063 W 0603
R821	1430069	Chip resistor	18 k	5 % 0.063 W 0603
R822	1430055	Chip resistor	6.8 k	5 % 0.063 W 0603
R823	1430167	Chip resistor	47	5 % 0.063 W 0603
R824	1430001	Chip resistor	100	5 % 0.063 W 0603
R826	1430063	Chip resistor	12 k	5 % 0.063 W 0603
R840	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R841	1430051	Chip resistor	4.7 k	5 % 0.063 W 0603
R842	1430049	Chip resistor	3.9 k	5 % 0.063 W 0603
R843	1430045	Chip resistor	2.7 k	5 % 0.063 W 0603
R844	1430009	Chip resistor	220	5 % 0.063 W 0603
R845	1430151	Chip resistor	10	5 % 0.063 W 0603
R846	1430001	Chip resistor	100	5 % 0.063 W 0603
R847	1430167	Chip resistor	47	5 % 0.063 W 0603
R863	1430015	Chip resistor	470	5 % 0.063 W 0603
C103	2310017	Ceramic cap.	22 n	10 % 100 V 0805
C104	2310017	Ceramic cap.	22 n	10 % 100 V 0805
C107	2310017	Ceramic cap.	22 n	10 % 100 V 0805
C108	2310017	Ceramic cap.	22 n	10 % 100 V 0805
C110	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C111	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C112	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C113	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C121	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C122	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C123	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C124	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C125	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C126	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C127	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C128	2320045	Ceramic cap.	27 p	5 % 50 V 0603

C129	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C130	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C131	2611668	Tantalum cap.	4.7 u	20 % 10 V 3.2x1.6x1.6
C132	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C133	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C134	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C135	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C136	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C137	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C138	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C139	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C140	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C141	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C142	2610105	Tantalum cap.	100 u	20 % 10 V 7.3x4.3x2.9
C144	2310009	Ceramic cap.	2.2 n	10 % 100 V 0805
C145	2517805	Electrol. cap.	47 u	20 % 100 V 10x10x10.5
C147	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C151	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C152	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C153	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C154	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C181	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C190	2517805	Electrol. cap.	47 u	20 % 100 V 10x10x10.5
C231	2310007	Ceramic cap.	18 n	10 % 100 V 1206
C232	2310007	Ceramic cap.	18 n	10 % 100 V 1206
C240	2310013	Ceramic cap.	100 n	10 % 100 V 1210
C251	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C252	2307816	Ceramic cap.	47 n	20 % 25 V 0805
C253	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C255	2310007	Ceramic cap.	18 n	10 % 100 V 1206
C256	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C260	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C261	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C270	2320067	Ceramic cap.	220 p	5 % 50 V 0603
C271	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C272	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C273	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C300	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C301	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C302	2604431	Tantalum cap.	10 u	20 % 16 V 6.0x3.2x2.5
C303	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C311	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C312	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C313	2610153	Tantalum cap.	10 u	20 % 6.0x3.2x2.5
C314	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C315	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C316	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C317	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206

C318	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C319	2610153	Tantalum cap.	10 u	20 % 6.0x3.2x2.5
C320	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C321	2610153	Tantalum cap.	10 u	20 % 6.0x3.2x2.5
C322	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C331	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C332	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C333	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C334	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C335	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C336	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C351	2610153	Tantalum cap.	10 u	20 % 6.0x3.2x2.5
C352	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C353	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C360	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C361	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C365	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C366	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C400	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C401	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C403	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C404	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C405	2320035	Ceramic cap.	10 p	5 % 50 V 0603
C406	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C407	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C408	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C409	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C410	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C412	2610013	Tantalum cap.	220 u	10 % 10 V 7.3x4.3x4.1
C413	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C414	2320107	Ceramic cap.	10 n	5 % 50 V 0603
C420	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C421	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C430	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C431	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C432	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C433	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C440	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C441	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C442	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C445	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C451	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C452	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C453	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C454	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C455	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C456	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C457	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206

C458	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C459	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C460	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C461	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C462	2320110	Ceramic cap.	10 n	10 % 50 V 0603
C501	2320011	Ceramic cap.	1.0 p	0.25 % 50 V 0603
C502	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C503	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C504	2320087	Ceramic cap.	1.5 n	5 % 50 V 0603
C505	2320011	Ceramic cap.	1.0 p	0.25 % 50 V 0603
C506	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C508	2320087	Ceramic cap.	1.5 n	5 % 50 V 0603
C509	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C511	2320051	Ceramic cap.	47 p	5 % 50 V 0603
C512	2320023	Ceramic cap.	3.3 p	0.25 % 50 V 0603
C513	2320023	Ceramic cap.	3.3 p	0.25 % 50 V 0603
C514	2320039	Ceramic cap.	15 p	5 % 50 V 0603
C515	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C516	2320019	Ceramic cap.	2.2 p	0.25 % 50 V 0603
C517	2320049	Ceramic cap.	39 p	5 % 50 V 0603
C518	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C519	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C520	2320043	Ceramic cap.	22 p	5 % 50 V 0603
C521	2320019	Ceramic cap.	2.2 p	0.25 % 50 V 0603
C522	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C530	2320015	Ceramic cap.	1.5 p	0.25 % 50 V 0603
C531	2320017	Ceramic cap.	1.8 p	0.25 % 50 V 0603
C532	2320017	Ceramic cap.	1.8 p	0.25 % 50 V 0603
C539	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C541	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C542	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C543	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C544	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C545	2320067	Ceramic cap.	220 p	5 % 50 V 0603
C546	2320067	Ceramic cap.	220 p	5 % 50 V 0603
C551	2320035	Ceramic cap.	10 p	5 % 50 V 0603
C552	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C553	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C554	2320464	Ceramic cap.	180 p	5 % 50 V 0603
C555	2320464	Ceramic cap.	180 p	5 % 50 V 0603
C556	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C557	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C558	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C559	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C560	2320091	Ceramic cap.	2.2 n	5 % 50 V 0603
C561	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C562	2320075	Ceramic cap.	470 p	5 % 50 V 0603
C563	2320051	Ceramic cap.	47 p	5 % 50 V 0603

C566	2320051	Ceramic cap.	47 p	5 % 50 V 0603
C569	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C570	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C571	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C572	2310791	Ceramic cap.	33 n	20 % 50 V 0805
C573	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C574	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C575	2320029	Ceramic cap.	5.6 p	0.25 % 50 V 0603
C580	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C600	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C601	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C602	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C603	2312410	Ceramic cap.	1.0 u	10 % 16 V 1206
C604	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C606	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C607	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C608	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C609	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C610	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C701	2320047	Ceramic cap.	33 p	5 % 50 V 0603
C702	2320023	Ceramic cap.	3.3 p	0.25 % 50 V 0603
C703	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C704	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C705	2320019	Ceramic cap.	2.2 p	0.25 % 50 V 0603
C710	2320031	Ceramic cap.	6.8 p	0.25 % 50 V 0603
C711	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C712	2320029	Ceramic cap.	5.6 p	0.25 % 50 V 0603
C713	2320023	Ceramic cap.	3.3 p	0.25 % 50 V 0603
C714	2320039	Ceramic cap.	15 p	5 % 50 V 0603
C715	2320023	Ceramic cap.	3.3 p	0.25 % 50 V 0603
C716	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C721	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C722	2320011	Ceramic cap.	1.0 p	0.25 % 50 V 0603
C724	2320021	Ceramic cap.	2.7 p	0.25 % 50 V 0603
C725	2320035	Ceramic cap.	10 p	5 % 50 V 0603
C726	2320011	Ceramic cap.	1.0 p	0.25 % 50 V 0603
C731	2320051	Ceramic cap.	47 p	5 % 50 V 0603
C733	2320019	Ceramic cap.	2.2 p	0.25 % 50 V 0603
C735	2320027	Ceramic cap.	4.7 p	0.25 % 50 V 0603
C736	2320015	Ceramic cap.	1.5 p	0.25 % 50 V 0603
C737	2320029	Ceramic cap.	5.6 p	0.25 % 50 V 0603
C738	2320027	Ceramic cap.	4.7 p	0.25 % 50 V 0603
C739	2320027	Ceramic cap.	4.7 p	0.25 % 50 V 0603
C740	2320055	Ceramic cap.	68 p	5 % 50 V 0603
C742	2320023	Ceramic cap.	3.3 p	0.25 % 50 V 0603
C743	2320025	Ceramic cap.	3.9 p	0.25 % 50 V 0603
C744	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C745	2320045	Ceramic cap.	27 p	5 % 50 V 0603

C746	2320027	Ceramic cap.	4.7 p	0.25 % 50 V 0603
C747	2320041	Ceramic cap.	18 p	5 % 50 V 0603
C752	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C753	2320055	Ceramic cap.	68 p	5 % 50 V 0603
C754	2320027	Ceramic cap.	4.7 p	0.25 % 50 V 0603
C755	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C756	2320033	Ceramic cap.	8.2 p	0.25 % 50 V 0603
C757	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C760	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C761	2320077	Ceramic cap.	560 p	5 % 50 V 0603
C762	2320055	Ceramic cap.	68 p	5 % 50 V 0603
C763	2320011	Ceramic cap.	1.0 p	0.25 % 50 V 0603
C764	2320055	Ceramic cap.	68 p	5 % 50 V 0603
C766	2320035	Ceramic cap.	10 p	5 % 50 V 0603
C767	2320021	Ceramic cap.	2.7 p	0.25 % 50 V 0603
C768	2320077	Ceramic cap.	560 p	5 % 50 V 0603
C770	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C771	2500708	Electrol. cap.	3300 u	20 % 16 V
C780	2320041	Ceramic cap.	18 p	5 % 50 V 0603
C781	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C782	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C783	2320045	Ceramic cap.	27 p	5 % 50 V 0603
C784	2320035	Ceramic cap.	10 p	5 % 50 V 0603
C785	2320035	Ceramic cap.	10 p	5 % 50 V 0603
C800	2604079	Tantalum cap.	0.22 u	20 % 35 V 3.2x1.6x1.6
C801	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C802	2320029	Ceramic cap.	5.6 p	0.25 % 50 V 0603
C803	2320067	Ceramic cap.	220 p	5 % 50 V 0603
C804	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C805	2320067	Ceramic cap.	220 p	5 % 50 V 0603
C806	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C807	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C809	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C814	2320027	Ceramic cap.	4.7 p	0.25 % 50 V 0603
C815	2313104	Ceramic cap.	1.0 n	2 % 50 V 1206
C817	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C818	2320053	Ceramic cap.	56 p	5 % 50 V 0603
C819	2320019	Ceramic cap.	2.2 p	0.25 % 50 V 0603
C823	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C824	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C825	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C826	2320095	Ceramic cap.	3.3 n	5 % 50 V 0603
C827	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C828	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C829	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C840	2320047	Ceramic cap.	33 p	5 % 50 V 0603
C841	2610100	Tantalum cap.	1 u	20 % 10 V 2.0x1.3x1.2
C843	2320045	Ceramic cap.	27 p	5 % 50 V 0603

C844	2320037	Ceramic cap.	12 p	5 % 50 V 0603
C845	2320041	Ceramic cap.	18 p	5 % 50 V 0603
C846	2320033	Ceramic cap.	8.2 p	0.25 % 50 V 0603
C847	2320027	Ceramic cap.	4.7 p	0.25 % 50 V 0603
C848	2320059	Ceramic cap.	100 p	5 % 50 V 0603
C849	2320083	Ceramic cap.	1.0 n	5 % 50 V 0603
C850	2320041	Ceramic cap.	18 p	5 % 50 V 0603
C851	2320049	Ceramic cap.	39 p	5 % 50 V 0603
C856	2320059	Ceramic cap.	100 p	5 % 50 V 0603
L101	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L102	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L103	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L104	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L130	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L131	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L141	3607551	Coil	125 u	10 % 2 A 16x12
L301	3606946	Ferrite bead 0.2r 26r/100mhz 1206		1206
L302	3606946	Ferrite bead 0.2r 26r/100mhz 1206		1206
L303	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L360	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L400	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L401	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L431	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L441	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L451	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L452	3640011	Filt z>600r/100m 0r6max 0.2a 0805		0805
L511	3641550	Chip coil	120 n	10 % Q=35/150 MHz 0805
L532	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L541	3641550	Chip coil	120 n	10 % Q=35/150 MHz 0805
L542	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L543	3641560	Chip coil	220 n	10 % Q=30/100 MHz 0805
L544	3641560	Chip coil	220 n	10 % Q=30/100 MHz 0805
L545	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L546	3608326	Chip coil	330 n	5 % Q=33/50 MHz 1206
L551	3641538	Chip coil	39 n	20 % Q=40/250 MHz 0805
L710	3645025	Chip coil	220 n	10 % Q=20/25 MHz 0805
L711	3641542	Chip coil	56 n	10 % Q=40/200 MHz 0805
L760	3606946	Ferrite bead 0.2r 26r/100mhz 1206		1206
L800	3641324	Chip coil	10 u	10 % Q=25/2.52 MHz 1008
L840	3641574	Chip coil	68 n	5 % Q=40/200 MHz 0805
L841	3641538	Chip coil	39 n	20 % Q=40/250 MHz 0805
B400	4510003	Crystal	32.768 k	+–20PPM 8x3.8
B800	4510075	Crystal	13.000 M	+–5PPM
G410	4700029	Battery cr2320 li 3v 130mah d23x2		D23X2
G810	4352933	Vco 1006–1031mhz4.5v 15ma dct2gsm		DCT2GSM
F100	5119002	SM, fuse f2.0a 32v	120	1206
Z500	4512046	Dupl 890–915/935–960mhz	37x14.7	37x14.7
Z501	4511016	Saw filter	947.5+–12.5 M	5.4x5.2

Z505	4511016	Saw filter	947.5+–12.5 M	5.4x5.2
Z541	4511026	Saw filter	71+–0.08 M	14.2x8.4
Z551	4510009	Cer.filt 13+–0.09mhz	7.2x3.2	7.2x3.2
Z713	4550101	Cer.filt 902.5+–12.5mhz	9.4x8.9	9.4x8.9
V101	4110053	Trans. supr.	82V	(SMB)DO214AA
V102	4110053	Trans. supr.	82V	(SMB)DO214AA
V103	4110053	Trans. supr.	82V	(SMB)DO214AA
V104	4110053	Trans. supr.	82V	(SMB)DO214AA
V121	4110074	Schottky diode	STPS340U	40 V 3 A SOD6
V122	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V123	4219926	Tr+rx2 rn1302 n50v50ma 10k sot323		SOT323
V125	4110015	Trans. supr.	8.2V	8.2 V DO214AA
V140	4211421	MosFet	RF1S9	p–ch 20 V TO263
V141	4210100	Transistor	BC848W	npn 30 V SOT323
V142	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V143	4115805	Diode	ES1C	ULTR A D0214AC
V146	4210106	Transistor	BSR19	npn 14 V 0.6 A SOT23
V170	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V202	4202671	MosFet	BST82	n–ch 80 V 175 mA SOT23
V203	4202671	MosFet	BST82	n–ch 80 V 175 mA SOT23
V205	4107160	Zener diode	BZX84	5 % 12 V 0.3 W SOT23
V206	4107160	Zener diode	BZX84	5 % 12 V 0.3 W SOT23
V212	4202671	MosFet	BST82	n–ch 80 V 175 mA SOT23
V213	4202671	MosFet	BST82	n–ch 80 V 175 mA SOT23
V215	4107160	Zener diode	BZX84	5 % 12 V 0.3 W SOT23
V216	4107160	Zener diode	BZX84	5 % 12 V 0.3 W SOT23
V221	4210106	Transistor	BSR19	npn 14 V 0.6 A SOT23
V222	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V223	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V224	4210106	Transistor	BSR19	npn 14 V 0.6 A SOT23
V225	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V226	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V240	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V250	4219926	Tr+rx2 rn1302 n50v50ma 10k sot323		SOT323
V300	4210020	Transistor	BCP69–25	pnp 20 V 1 A SOT223
V302	4219926	Tr+rx2 rn1302 n50v50ma 10k sot323		SOT323
V303	4210100	Transistor	BC848W	npn 30 V SOT323
V304	4210100	Transistor	BC848W	npn 30 V SOT323
V341	4219926	Tr+rx2 rn1302 n50v50ma 10k sot323		SOT323
V401	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V402	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V403	4110072	Diode x 2	BAV99W	70 V 0.2 A SOT323
V404	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V422	4219926	Tr+rx2 rn1302 n50v50ma 10k sot323		SOT323
V423	4219926	Tr+rx2 rn1302 n50v50ma 10k sot323		SOT323

V424	4219926	Tr+rx2 rn1302 n50v50ma 10k sot323		SOT323
V425	4219926	Tr+rx2 rn1302 n50v50ma 10k sot323		SOT323
V426	4102998	Led	Green	2.2 V 1206
V427	4102998	Led	Green	2.2 V 1206
V428	4102998	Led	Green	2.2 V 1206
V429	4102998	Led	Green	2.2 V 1206
V430	4210108	Transistor	BSR20	pnp 12 V 0.6 A SOT23
V431	4210108	Transistor	BSR20	pnp 12 V 0.6 A SOT23
V501	4210074	Transistor	BFP420	npn 4. V SOT343
V502	4210074	Transistor	BFP420	npn 4. V SOT343
V503	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V504	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V505	4210100	Transistor	BC848W	npn 30 V SOT323
V506	4210100	Transistor	BC848W	npn 30 V SOT323
V511	4115802	Sch. diode x 2	4V	30 mA SOT23
V512	4210046	Transistor	BFP182	npn 20 V 35 mA SOT143
V541	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V601	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V701	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V702	4100567	Sch. diode x 2	BAS70–04	70V15 mA SERSOT23
V720	4200755	Transistor	BFR92A	npn 15 V 25 mA SOT23
V730	4200755	Transistor	BFR92A	npn 15 V 25 mA SOT23
V731	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V740	4210090	Transistor	BFG540/X	npn 15 V 129 mA SOT143
V741	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V750	4210133	Transistor	BFG10W/X	npn 10 V 0.25 A SOT343
V751	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V760	4210135	Transistor	BLT82	npn 10 V SO8S
V761	4210100	Transistor	BC848W	npn 30 V SOT323
V772	4217070	Transistor x 2		IMD
V773	4210100	Transistor	BC848W	npn 30 V SOT323
V775	4210100	Transistor	BC848W	npn 30 V SOT323
V781	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V791	4100285	Diode x 2	BAV99	70 V 200 mA SER.SOT23
V800	4111092	Cap. diode	BB639	30 V SOD323
V801	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V802	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V840	4110018	Cap. diode	BB135	30 V SOD323
V841	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
V842	4210066	Transistor	BFR93AW	npn 12 V 35 mA SOT323
D360	4370133	IC, tms320lc546 3v wd4	tqfp1 DSP	TQFP100
D400	4370101	Cf70131 gsm/pcn asic bart sqfp144		SQFP144

D410	4303679	IC, 4 x nand	74HC00	SO14
D420	4340307	IC, MCU		TQFP80
D430	4340217	Te28f008s3 flash 3.3v 1mx8 tsop40		TSOP40
D440	4340333	IC, SRAM		TSOP32
D445	4343280	IC, EEPROM		2kx8 bit SO8S
N130	4370301	St5092 pcm codec/filter so28		SO28
N140	4305236	IC, 2 x comp.	LM2903	SO8S
N250	4340215	Am79r79 subscrib.interface plcc32		PLCC32
N300	4370223	Stt261c pscld_e pw supply tqfp44		TQFP44
N350	4301062	IC, regulator	LP2951AC	SO8S
N450	4370097	St7523 rfi2 v4.2 tdma codec qfp64		QFP64
N551	4370243	Crfrt_st tx.mod+rxif+pwc sqfp44		SQFP44
N601	4370095	Crfcontf 8xreg4.5v vref2v5 vsop28		VSOP28
N820	4340005	IC, 2xsynth 1.2ghz 3v sso	UMA1018M	SSO20
S410	5200914	Push button switch 2–pole 6x7 smd		SMD
X100	5409043	SM, modular jack 6pol right angl		ANGLE
X101	5409043	SM, modular jack 6pol right angl		ANGLE
X110	5414943	Dc–jack d6.3/2 pcb		
X120	541Y001	PCB connector 2x10 2.54p horizont.smd		HORIZONT.SMD
X300	5408807	Sim card reader ccm04–5002 2x		3CO2x3con
X500	5420011	Connector mini uhf 90’deg <2.5gh		<2.5GHZ
X510	5420011	Connector mini uhf 90’deg <2.5gh		<2.5GHZ
	9854267	PCB WT4C 202.0X110.0X1.6 M4 1/PA		
	9854267	PC board WT4C 202.0x110.0x1.6 m4 1/pa1/PA		

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